Keysight
N4960A Serial BERT 17 and 32 Gb/s

Data Sheet

Affordable characterization and manufacturing test solution for transceivers up to 32 Gb/s

16GFC, 32GFC, 100G Ethernet, InfiniBand FDR, InfiniBand EDR, and Fast SERDES

KEYSIGHT
TECHNOLOGIES

Product highlights

– Full data rate pattern generation and error detection
– Integrated clock source with calibrated stress capability
– Built-in selection of PRBS and common telecom/datacom test patterns
– Fully programmable user-defined patterns
– Remote heads place the signal very close to DUT

Solving the need for speed... Without breaking your budget

Verifying 100G ethernet or 16GFC transceivers requires a BERT operating beyond 13G. This often results in multiple designers needing to share the one serial BERT in the lab—delaying their characterization, along with the development schedule.

The N4960A BERT has fast transition times and real time BER count updates. In addition, low intrinsic jitter provides continuously settable clock frequencies allowing data rates from 5 to 32 Gb/s rates and from 4 to 17 Gb/s. As a result, high quality signals produce excellent fidelity in the eye for improved measurement accuracy.

The solution is compact—allowing it to be easily transported throughout the lab and manufacturing.

Compact architecture

The N4960A serial BERT system consists of the N4960A clock source/controller plus remote pattern generator (N4951A/B) and error detector (N4952A) heads. The controller can operate as a stand alone clock source, with jitter injection, in addition to providing the precision timing and control required for remote pattern generator and error detector heads.

Place signal close to DUT

The concept of remote heads, first introduced with the N4965A multi-channel BERT controller, puts the pattern generation and error detection near the device under test, eliminating long cables which degrade the signal. This is especially important beyond 17 Gb/s.

Figure 1. Place signal close to DUT.

Integrated 32 Gb/s operation

Pattern generator and error detector remote heads are available in two data rate verions:
- 17 Gb/s versions operate over 4 to 17 Gb/s
- 32 Gb/s versions operate over 5 to 32 Gb/s

Both versions operate over their entire band with no gaps or missing data rates. The numbers 17 or 32 form the last two digits of the model/option number and indicate the data rate range of the remote head. For example,
- N4951A-P32 pattern generator operates over 5 to 32 Gb/s;
- N4952A-E17 error detector operates over 4 to 17 Gb/s

The remote heads generate and test full rate patterns directly without the need for external multiplexers and delay matching. Each includes a selection of PRBS pattern lengths, along with a large selection of common telecom, datacom, and clock stress test patterns including K28.5, CJPAT, CJTPAT, JSPAT, JTSPAT, etc.

Pattern generator heads are available in N4951A and N4951B models.

The signal fidelity in the eye is outstanding. Output parameters of amplitude, offset, and termination voltage are user settable.
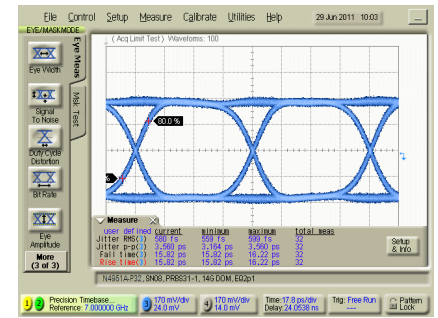
Each N4960A controller can support
0 remote heads
1x pattern generator head only
1x error detector head only
1x pattern generator and 1x error detector head
2x pattern generator heads

Complete, compact, flexible configurations 17 Gb/s and 32 Gb/s BERT

Does your application need a full BERT? Keysight offers a surprisingly affordable total solution which includes both pattern generation and error detection capability. Tied together with our N4980A multi-instrument BERT software, this combination provides a powerful BERT solution.

Of course, the system also operates without the error detector or pattern generator, for applications which require these configurations.

Alternatively two pattern generators can be connected to a controller with programmable delay skew control between the generators for use in I-Q modulator applications.

Figure 2. Typical eye at 14 Gb/s.

N4951B-H17/-H32 pattern generator high amplitude remote head

The N4951B-H17/-H32 provides 6 V differential outputs suitable for directly driving VCSELs, TOSAs and optical modulators without the need for external amplifiers. In addition to eliminating the need for extra signal connections and power supplies, integrating the higher voltage driver inside the pattern generator allows direct amplitude control from the same user interface with the other pattern generator controls.
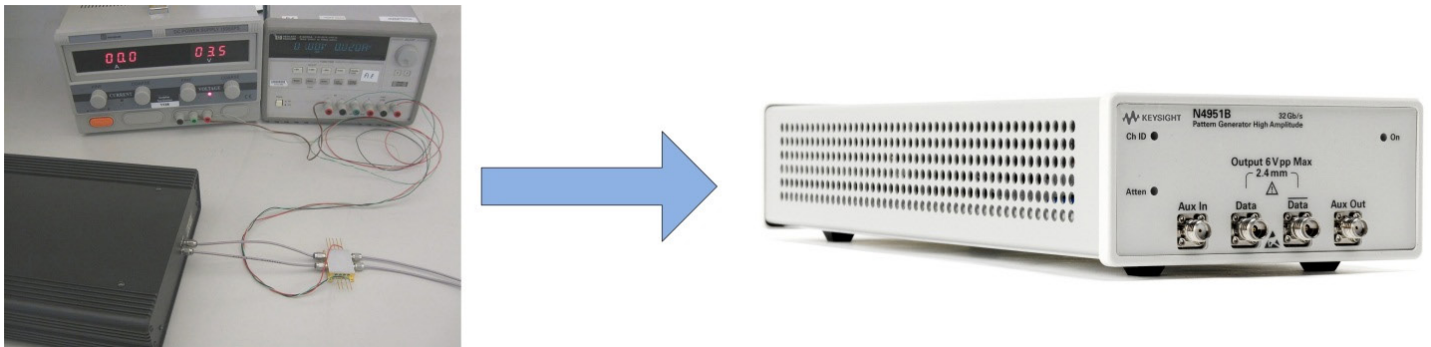

Figure 3. External amplifier with external power supply versus the N4951B-H17/-H32.

The N4951B pattern generator also features improved rise/fall times and lower intrinsic jitter performance to meet the needs of today's characterization requirements in server, line card, backplane and communications IC applications.
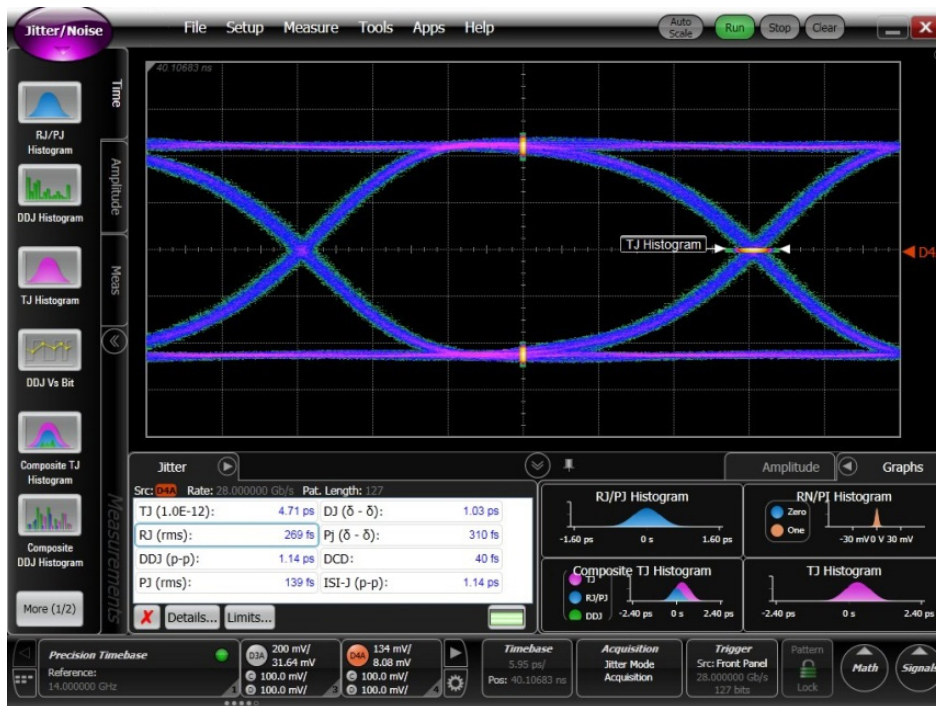

Figure 4. N4951B-H32 output at 28 Gb/s 6 V p-p differential.

N4951B-D17/-D32 pattern generator with 5-tap de-emphasis remote head

The N4951B-D17/-D32 de-emphasis options provide integrated 5-tap de-emphasis (1 pre-cursor, 3 post cursors) and are available in 17 Gb/s and 32 Gb/s versions. The de-emphasis head provides designers with the signal pre-distortion capability required for transmitter emulation and equalization when characterizing receivers, backplanes, and systems.
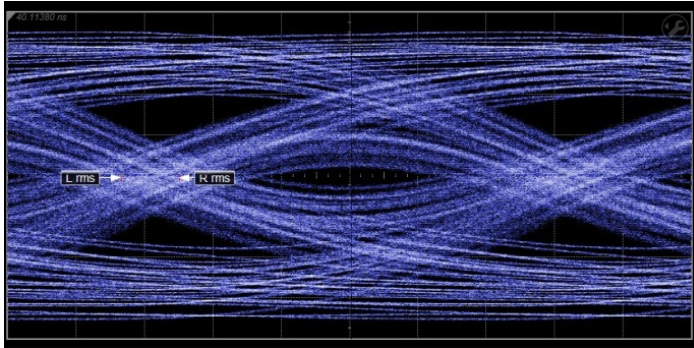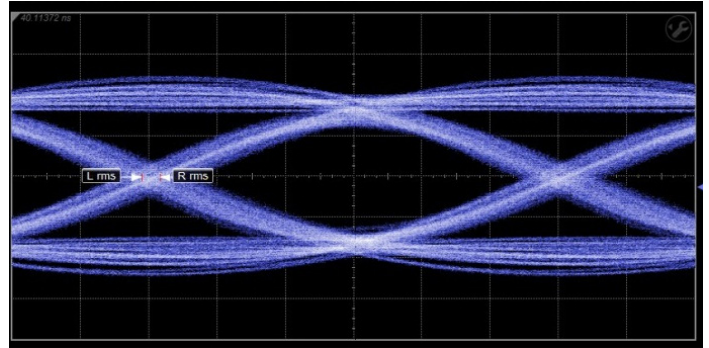

Figure 5. No de-emphasis.

Figure 6. De-emphasis equalization applied.

Simplify tap weight computation

The N4980A Multi-instrument BERT software includes a powerful de-emphasis tap weight computation tool that simplifies the process of computing tap weights, reducing the time required to a few seconds. Starting from a measured or simulated S-Parameter file of the data path to be equalized, the software calculates the optimum tap values necessary to create the ideal compensation filter response. The user can control tap configurations, so different solutions with different ranges of pre- and post-cursors can be synthesized. Once the data has been analyzed and desired results obtained, a single click loads the computed tap weights directly into the N4951B-D17/-D32 pattern generator head.

Figure 7. De-emphasis tap weight calculator.

Choose the complement of stress sources you need

The controller is offered in two versions. The N4960A-CJ0 is the base model and is ideal for many optical serial data applications, providing a single tone of sinusoidal jitter injection. Settable over a wide range of frequencies and modulation depth, it facilitates jitter tolerance testing and general receiver characterization.

For applications which require a more complex "stress recipe", the N4960A-CJ1 includes two independent sources of sinusoidal along with broadband true random jitter sources. The multiple stress generators allow you to build a low level base floor that is a mixture of random and possibly sinusoidal jitter. In addition, all clock outputs can be modulated with spread spectrum, with a deviation settable up to 1.0 % of the clock frequency (10,000 ppm).
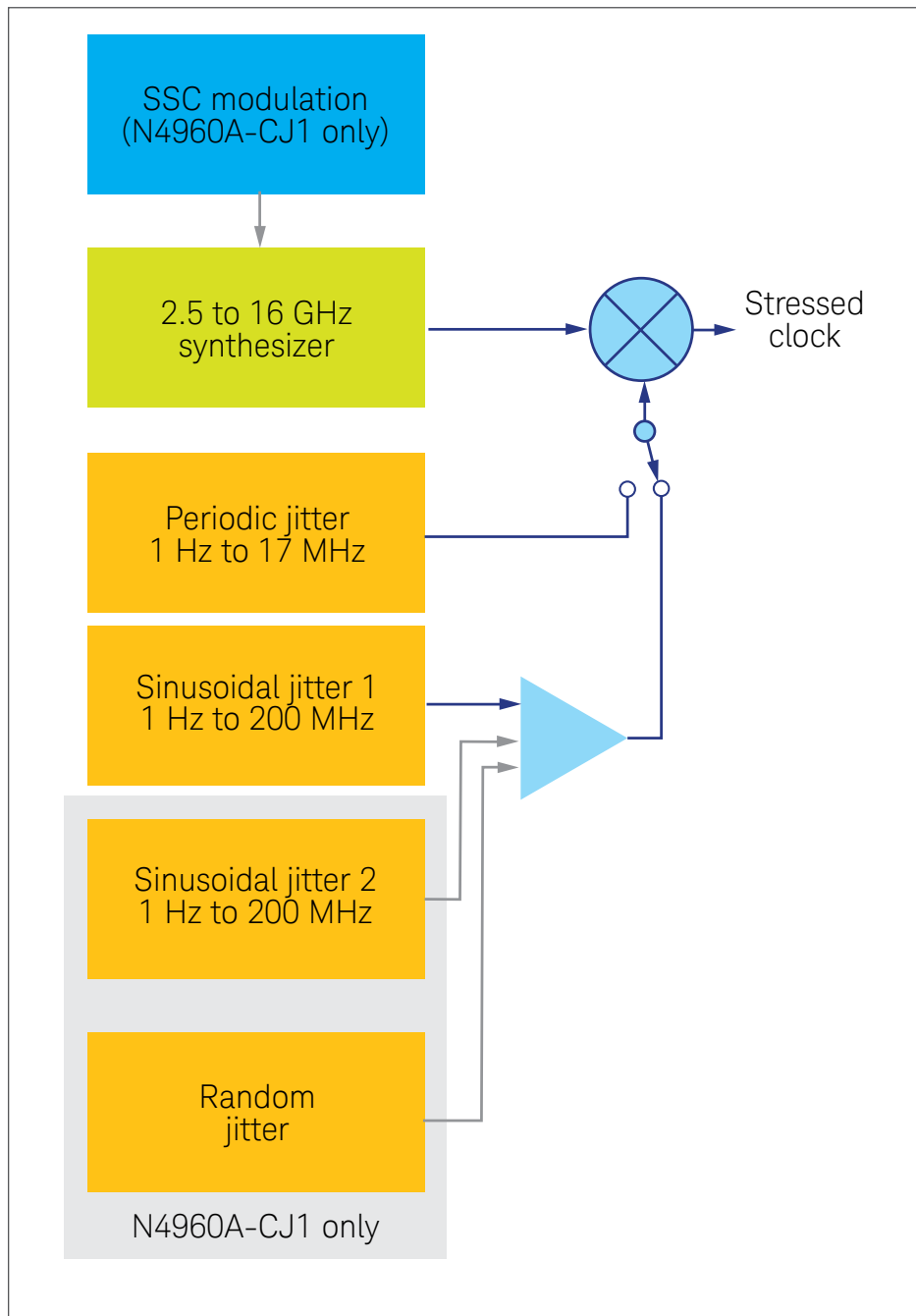

Figure 8. Stress sources.

Integrated control interface and analysis software

Support for the N4960A serial BERT is included in the N4980A multi-instrument BERT software. The base software provides an intuitive user interface and is free of charge. With the base software, you can perform single-channel BER, multi-channel BER with an unlimited number of channels, and bathtub measurements. Measurement results can be plotted or saved, as well as complete test setups. The optional jitter tolerance package adds single and multi-channel JTOL measurements with a choice of search algorithms. Testing JTOL in multi-lane devices in parallel is much faster than testing each lane individually, and more representative of the actual operating environment with live traffic present on all lanes. With the JTOL template editor, you can create templates to meet the testing criteria of the most common standards. The JTOL package requires a license to use.

The N4980A multi-instrument BERT software also facilitates the setup and execution of multi-channel BER measurements. The Multi-channel N4960A control window supports up to 4x N4960A BERTs allowing for easy setup and instrument control during synchronous or asynchronous channel testing in 100GbE applications.

Figure 9. N4980A multi-instrument BERT software.

Figure 10. N4980A multi-channel BER measurement interface.

Figure 11. N4960A multi-channel hardware configuration.

Programmable patterns

For special pattern requirements, programmable patterns up to 8 Mb in length can be easily created with powerful editing tools built into the N4980A multi-instrument BERT software. Patterns can then be uploaded into the N4960A serial BERT controller.

The programmable pattern editor is used to create and manage pattern streams. Pattern streams are composed of one or more sub-patterns. Each sub-pattern contains a single pattern definition. Using sub-patterns allows users to break down complex patterns for easier organization.

Sub-patterns can be edited at the bit level using the edit pattern dialog box. In this dialog box, users can create, view, edit, and find specific bit sequences.

Once the pattern definition is complete, it can be validated and uploaded to the N4960A serial BERT controller. It can also be saved to the PC as a *.cpf file.

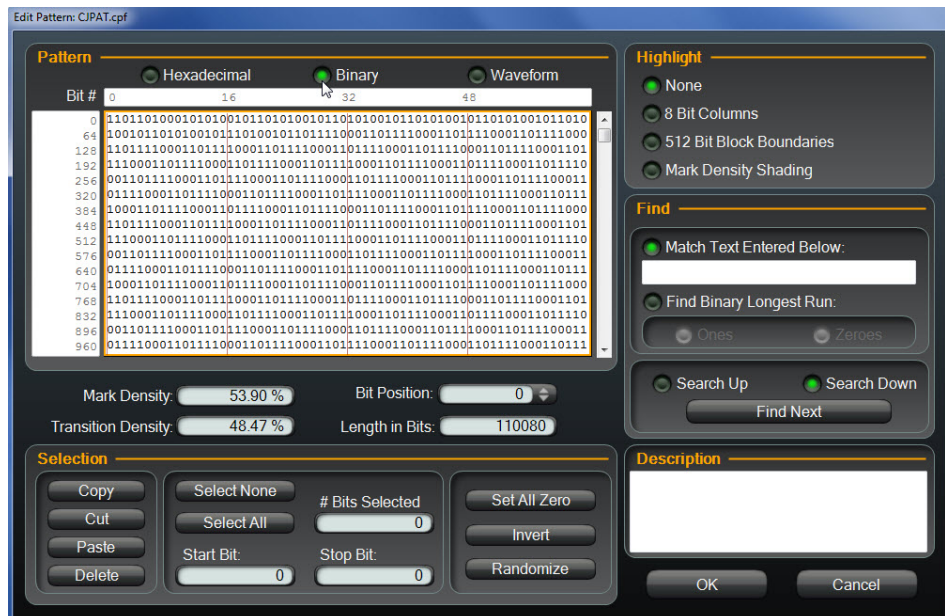Figure 12. Programmable pattern editor.

Figure 13. Sub-pattern editor.

General purpose serial data clock source

In addition to being a BERT solution, the N4960A serial BERT controller is a clock synthesizer. The N4960A can be used with other non-stressed BERTs to provide jitter capability. You can also use it for general purpose serial data characterization applications. When used as a BERT by attaching the pattern generator and error detector remote heads, the BERT settings override the settings for the clock outputs.

Three clock outputs

A traditional BERT setup uses a stressed (jittered) clock source for the pattern generator and a clean (non–jittered) clock for the error detector. The phase delay between these clocks must be adjustable in fine resolution of time to center the error detector sample point in the eye. The N4960A serial BERT controller has dedicated outputs for both jittered and delayed signals. In addition, a clean divided clock output is provided for applications requiring a sub rate reference, or as a trigger for sampling oscilloscopes.

Each output is configured as a differential signal but can be used single ended without the need to terminate the unused output. To address the requirements of any application, the amplitude, offset voltage, termination voltage, and coupling can be independently set on each of the three outputs.

Two independent SJ sources (single source in N4960A-CJ0 serial BERT controller)

For the N4960A serial BERT controller the stress source choices are one (N4960A-CJ0) or two (N4960A-CJ1) tones of high frequency sinusoidal jitter (SJ) with user settable frequency and amplitude (phase deviation). The SJ sources are summed with random jitter and any externally applied high band jitter. The frequency range of the two SJ sources is 1 Hz to 200 MHz with a modulation range of up to 1.0 UI.

Figure 14. Clock outputs.

High deviation PJ source

A separate modulation path is available for low frequency (high deviation) stress injection. This path is operated when all of the high frequency band (low deviation) stress sources (SJ1, SJ2, RJ, and external low deviation) are disabled. The low band path operates over lower modulation frequencies, up to 17 MHz (using internal PJ), or up to 4 MHz (external). The modulation source can be either an internally generated sinusoid (periodic jitter, or PJ), or externally supplied through the "Ext Jitter In" connector.

True random jitter source (N4960A-CJ1 serial BERT controller)

The RJ source provides true Gaussian random jitter with a crest factor of at least 14. The unfiltered spectral content is flat from DC to the contour of the high frequency band modulator, which has –3 dB BW at approximately 320 MHz. For applications which require a specified RJ frequency contour, an external filter can be placed in the RJ modulation signal path. Both a low pass and a high pass filter can be used in series when both ends of the spectrum require filtering.

The RJ modulation is calibrated with no filters in the path. However, if a filter is inserted in the RJ path, then the modulation amplitude will be attenuated from the calibrated value due to the filter attenuation.

Spread spectrum clock (N4960A-CJ1 serial BERT controller)

The main synthesizer in the N4960A-CJ1 serial BERT controller can be modulated to enable spread spectrum clocking (SSC). Spread spectrum clocking is not generally considered to be a stress, but rather a method of controlling electromagnetic interference (EMI), by spreading the peak energy of the system clock over a broad portion of the spectrum. In practice, SSC modulates the system clock in the device with a large phase deviation at a relatively low frequency, generally 30 or 33 kHz. The modulation wave shape is usually a triangle wave, to keep the power spectrum even over the modulation band. SSC is included in clock synthesizers used in BERTs to emulate a transmitter from a device which employs SSC. To assure proper tracking of the BERT or sampling scope testing a device with SSC, all three clock outputs of the N4960A-CJ1 (jittered, delayed and divided) are modulated with the same SSC signal. The SSC deviation range is 0 to 1% (1% = 10,000 ppm). The modulation envelope is a triangle waveform. The modulation frequency can be set from 1 Hz to 50 kHz. In addition, there are three settings for deviation direction: down, center, and up (relative to the clock frequency setting).

Large library of common stress patterns

The N4960A serial BERT controller comes with a library of stress patterns including PRBS, divided clock, JSPAT, JTSPAT, K28 series, and CJ series for optical telecom and datacom testing.

Jitter tolerance testing

Keysight provides an affordable solution for testing jitter tolerance. The N4980A multi-instrument BERT software saves you time and money by providing a way to efficiently test jitter tolerance.

The optional JTOL measurement package (N4980A-JTS) performs jitter tolerance compliance and characterization. Setup is quick and easy using the jitter tolerance setup panel.

Figure 15. Jitter tolerance setup panel in N4980A.

BER measurement results of each tested sinusoidal jitter point can be displayed in graphical format. A green colored dot on the graph at right indicates the point at which the receiver is passing, a red colored X indicates a synchronization issue, and the maroon colored + sign indicates the point at which the BER threshold has been exceeded.

The x-axis of the graph is PJ/SJ frequency and the y-axis is PJ/SJ amplitude. The compliance template is shown with a dashed line. The minimum and maximum bounds for the characterization test are shown with a solid line.

The results can also be displayed in tabular format (Figure 17) and can be saved to a file for future analysis.

The jitter amplitude and frequency test points are defined in a template file which can be edited by simply pointing and clicking a mouse or entering the information in the numeric fields (Figure 18).
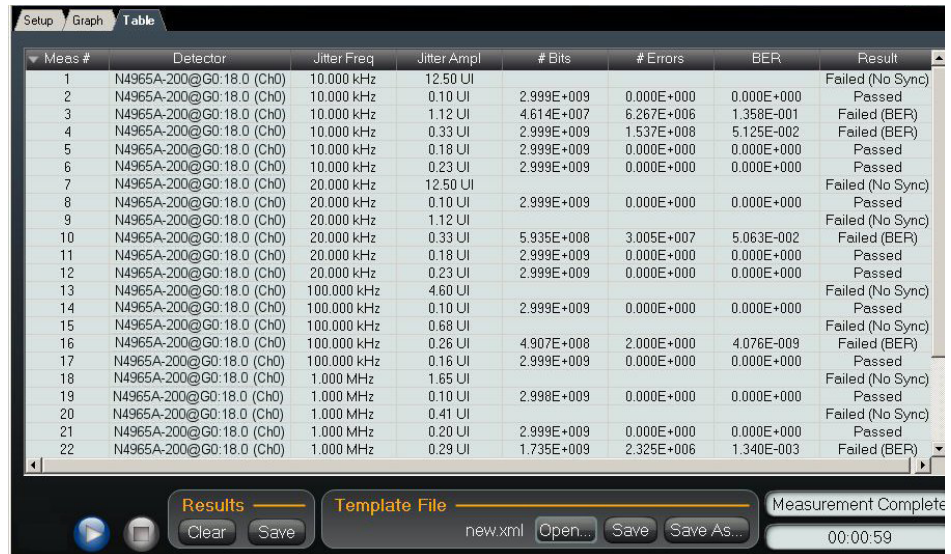

Figure 16. Jitter tolerance graph view.

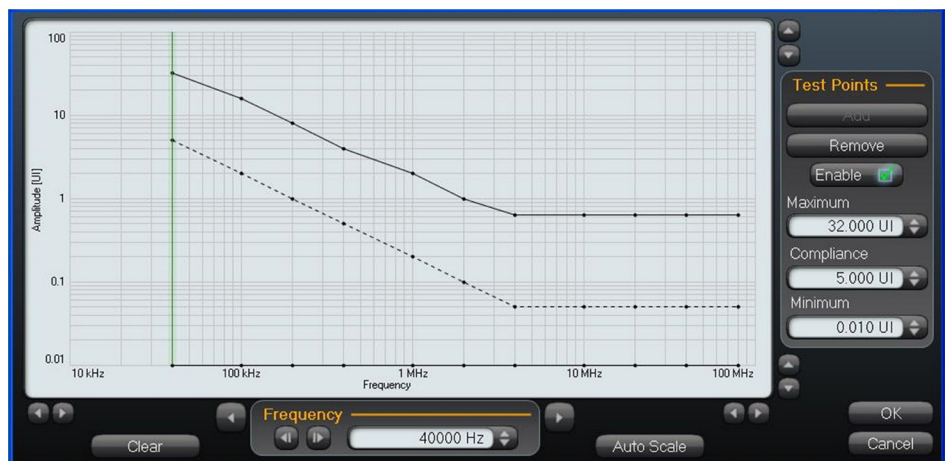Figure 17. Jitter tolerance table view.

Figure 18. Template file.

Typical applications

100G ethernet

The 100G Ethernet is the next generation 25 Gb/s standard for evaluating chip-to-chip and chip-to-module electrical communication links within optical networks.

The example configuration below (Figure 19) requires four 25 Gb/s lanes. This is accomplished using four 32 Gb/s pattern generators (N4951A-P32 or N4951B-H32/-D32) to the input of the optical module. The optical module is tested in loopback mode with the receiver's electrical outputs connected to four 32 Gb/s error detectors.

This configuration supports asychronous clocking on all 4 lanes, which is required for characterizing 100GE-SR4 system components.
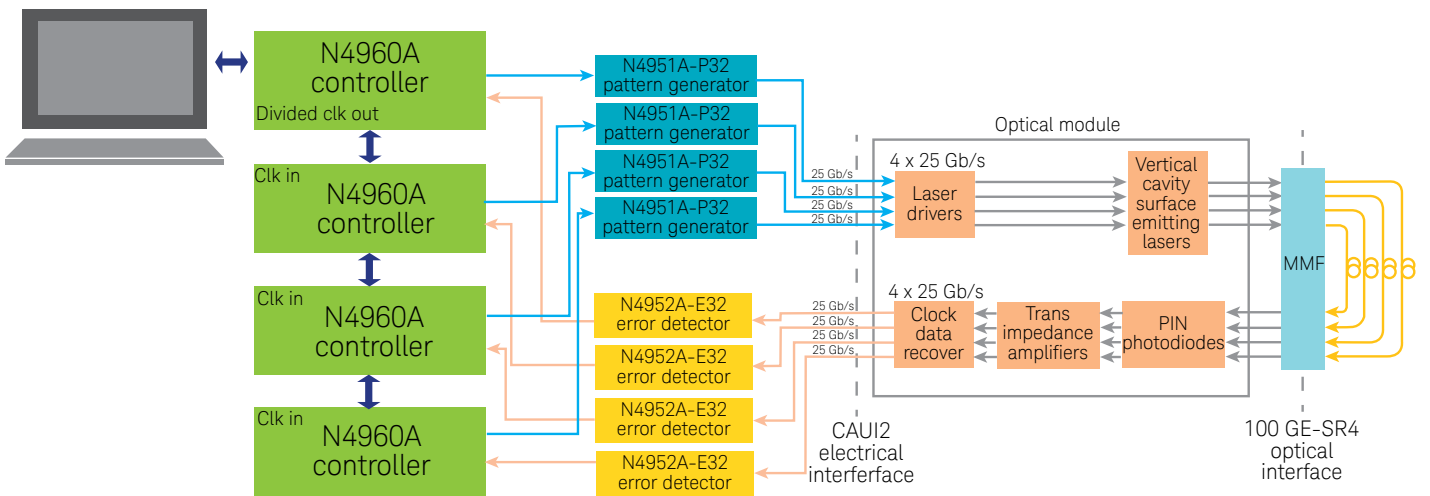
Figure 19. Test setup for 100G ethernet.

Fast SerDes design in FPGA and other communication ICs

SerDes circuits are often integrated into the design of FPGAs, ASICs, and other communication ICs. To ensure successful integration, SerDes circuits must be fully tested and characterized before integration.

Figure 18 shows a configuration for testing the received data through a loopback in a SerDes. The BER and jitter tolerance can be measured at all rates up to 32 Gb/s using the N4960A serial BERT on the transmit side of a SerDes.

The pattern editor in the N4980A multi-instrument BERT software enables the design of stress patterns and pattern streams for the specific application. In addition, the software simplifies the task of setting up and running BER and jitter tolerance tests.
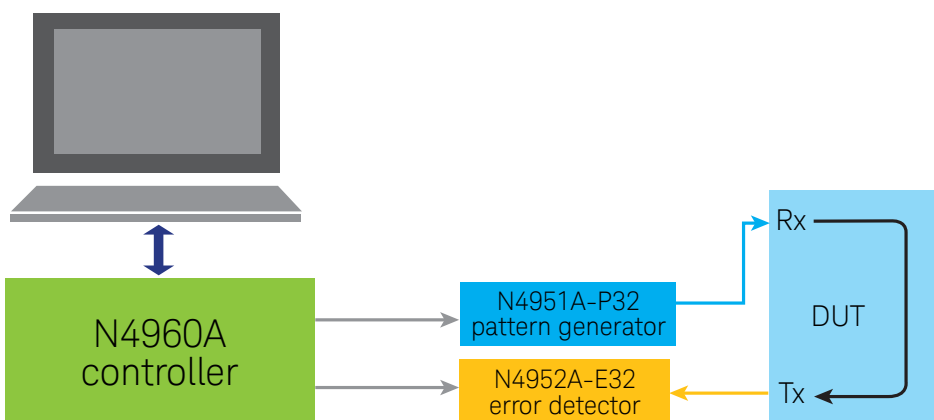
Figure 20. Test setup for communication ICs.

16GFC

Testing 16GFC devices requires equipment capable of 14.025 Gb/s. Used in the storage, computing, and communications industries, 16GFC devices must be accurately character-ized to strict tolerances.

A basic configuration using the
17 Gb/s BERT system is shown above. N4951A-P17 (or N4951B-H17/-D17) and
N4952A-E17 can be loaded with common stress patterns for 16GFC. You can also custom design your own patterns up to 8 Mb in length and upload them into the N4960A serial BERT.

Figure 21. Test setup for 16GFC.

Block diagram 32 Gb/s serial BERT

Figure 22. Block diagram (32 Gb/s system).

Block diagram 17 Gb/s serial BERT

Figure 23. Block diagram (17 Gb/s system).

Configuration guide

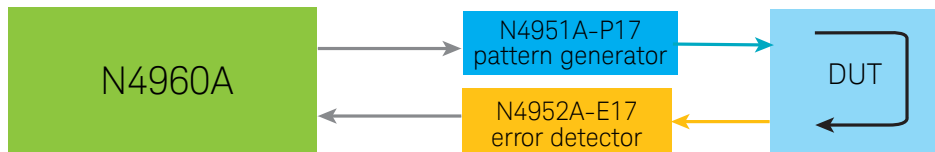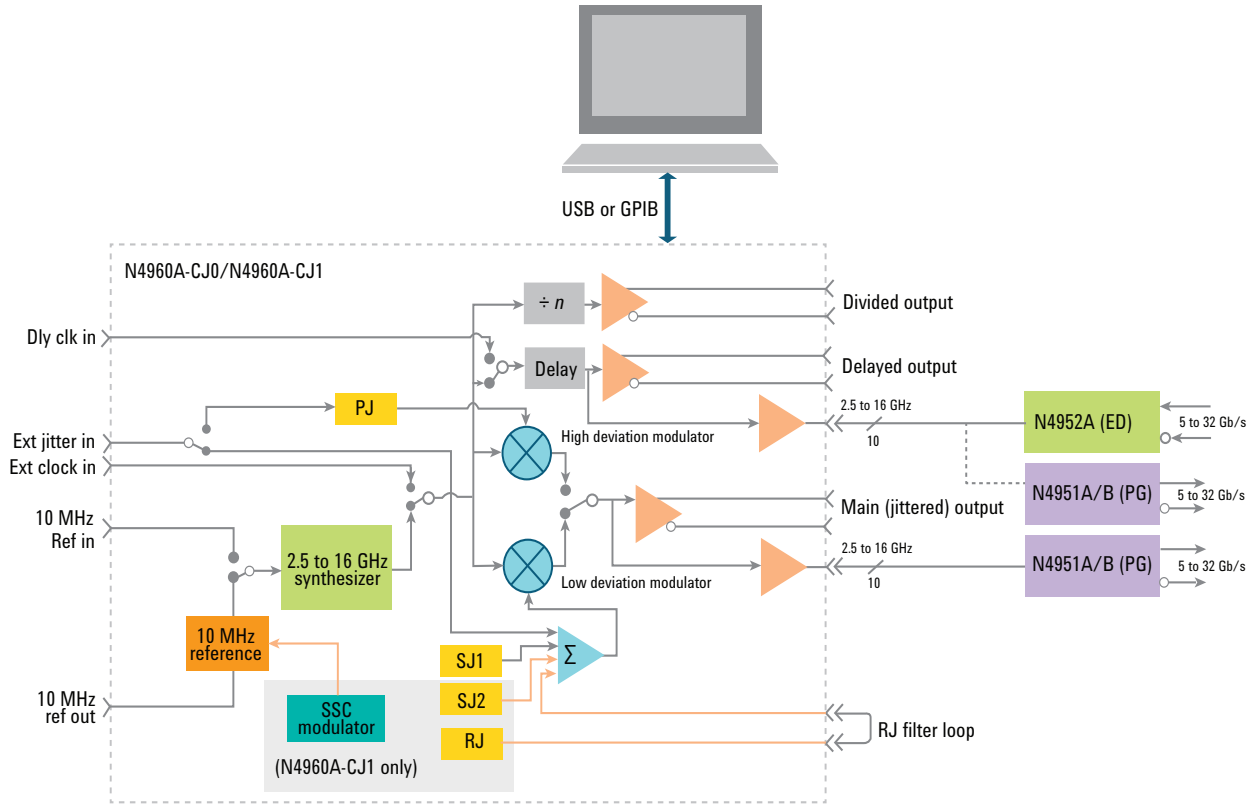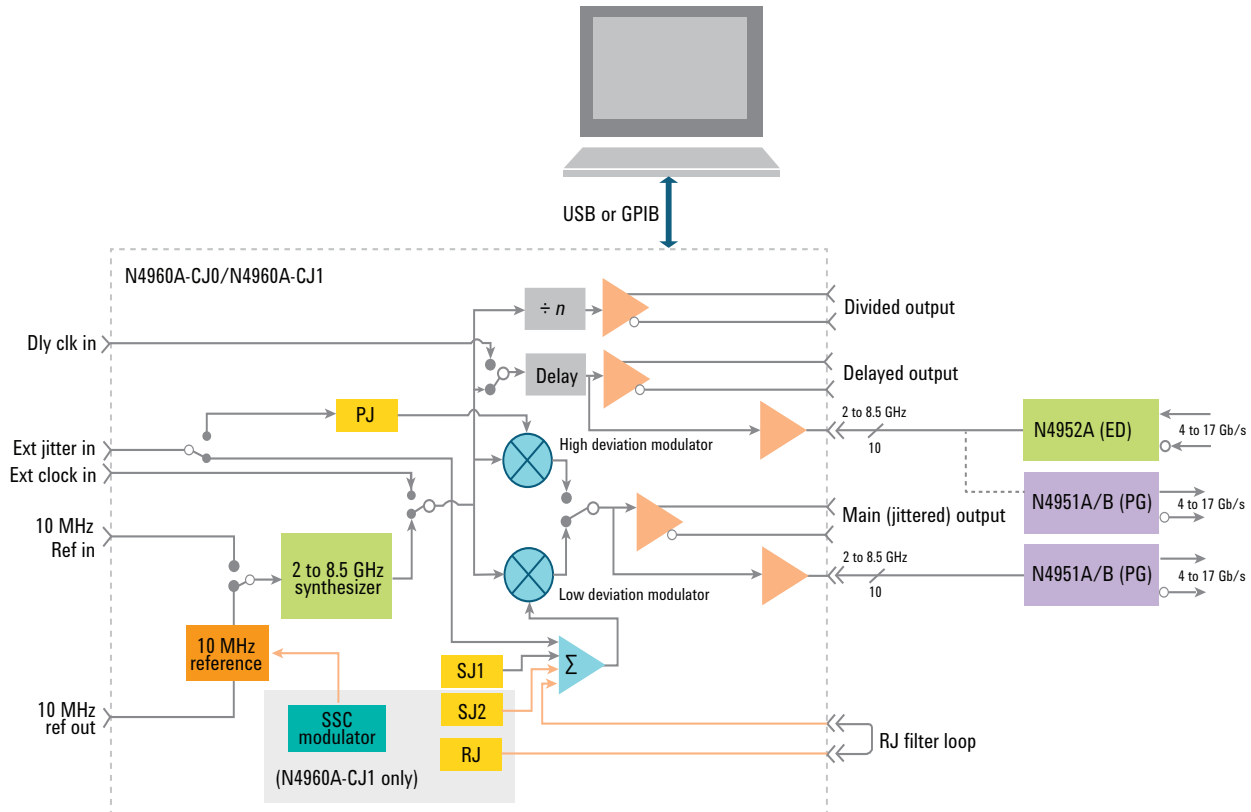**Step 1. Select the controller**

Description	N4960A-CJ0	N4960A-CJ1
Periodic jitter	√	√
Single tone sinusoidal jitter	√	√
Multi-tone sinusoidal jitter		√
Random jitter		√
Spread spectrum clock		√

Step 2. Select the pattern generator(s)[1]

Description	N4951A		N4951B		N4951B	
	P17	P32	H17	H32	D17	D32
Data rate, 4 to 17 Gb/s	√		√		√	
Data rate, 5 to 32 Gb/s		√		√		√
Data output connectors, 2.92 mm	√	√				
Data output connectors, 2.4 mm			√	√	√	√
Output amplitude, single-ended, max 1.0 V (p-p)	√	√				
Output amplitude, single-ended, max 1.5 V (p-p)					√	√
Output amplitude, single-ended, max 3.0 V (p-p)			√	√		
Rise time (20% to 80%), 15 to 17 ps typical	√	√			√	√
Rise time (20% to 80%), 12 ps typical			√	√		
5 tap de-emphasis					√	√

1. A second pattern generator may be selected that connects to the N4960A Delay connector.

Step 3. Select the error detector

Description	N4952A-E17	N4952A-E32
Data rate, 4 to 17 Gb/s	√	
Data rate, 5 to 32 Gb/s		√

Step 4. Select optional software

Description	Model Number
Multi-instrument BERT software	N4980A
Jitter tolerance software package	N4980A-JTS

N4960A clock source/BERT controller specifications

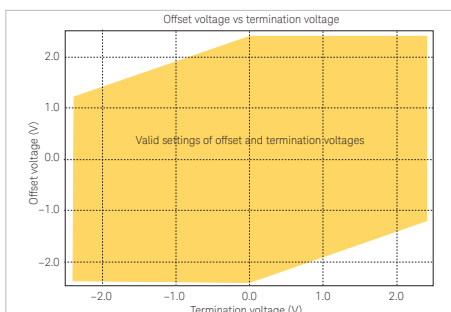|	
Configuration	Frequency synthesizer with three differential outputs: Jitter, Delay, and Divided. Clock generator Jitter and Delay clocks are shared with the remote head port connectors. Changing the controller clock output parameters while pattern generator and/or error detector remote heads are operating will effect their operation. Pattern generator and error detector remote heads operate with a half-rate clock - therefore the remote head Data rate will be double the frequency of the controller Clock.
Frequency	1 to 16 GHz with no remote heads connected
	2 to 8.5 GHz when one or two 17 Gb/s remote heads are connected
	2.5 to 16 GHz when one or two 32 Gb/s remote heads are connected
Frequency resolution	1 kHz (front panel)
Outputs	Jitter (stressed), Delay, and Divided (non-stressed)
Output configuration (all outputs)	Differential, with amplitude, offset and termination voltage adjustment (can be used single-ended without terminating unused outputs)
Amplitude range	300 mV to 1.7 V (p-p), single-ended
Offset range	–2.4 to +2.4 V (limited by termination voltage, see Figure 24)
	On divided clock output, this is only valid when the divide ratio is a power of 2.
Termination voltage range	–2.4 to +2.4 V (limited by offset voltage, see Figure 24)
Rise time (20% to 80%)	< 23 ps typical
Intrinsic jitter	< 700 fs rms typical from 2 to 16 GHz
Duty cycle	
Jitter and delay outputs	50% ±5%
Divided output	50% ±5% at divide ratios which are a power of 2
	Duty cycle varies between 33 and 66% at divide ratios which are not a power of 2
	50% ±10% when divide ratio is set to 1 for amplitudes ≥ 500 mV
Frequency accuracy	± 1 ppm typical, ± 5 ppm maximum
Reference frequency	10.0 MHz, single-ended output and input on rear panel
External clock	Single-ended input can be substituted for internal synthesizer, drives all clocks
Maximum clock input amplitude	2 V (p-p)
Clock input sensitivity	200 mV typical
External delayed clock input	Single-ended input drives Delay clock outputs only
Maximum delayed clock input amplitude	2 V (p-p)
Delayed clock input sensitivity	150 mV typical
Spread spectrum clock (N4960A-CJ1 serial BERT controller only)	Phase deviation appears on all outputs (internal synthesizer only)
Deviation range	0 to 1.0% (10,000 ppm)
Modulation frequency range	1 Hz to 50 kHz
Modulation wave shape	Triangle
Deviation direction	Down spread, center spread, or up spread
Divided clock divide ratio	÷ 1, 2, 3,…, 99,999,999, with no missing integers (waveshape of divided clock slower than ≈1 MHz will be differentiated)
Delayed clock delay range	0 to ±1,000 UI
Delayed clock delay resolution	1 mUI
Connector type	
All signals except 10 MHz ref in/out	SMA
10 MHz ref in, out	BNC

Figure 24. Maximum offset and termination voltage ranges.

N4960A clock source/BERT controller jitter specifications

Configuration	Calibrated stress is added to Jitter Clock Output and the Jitter remote head port clock through one of two modulators: a high deviation, low frequency path, or a low deviation, high frequency path. The amplitude of any stress appearing on the front panel Jitter Clock Output will be 1/2 of the value appearing at the N4951A/B remote head pattern generator data output (if connected to the Jitter port). Changing stress amplitudes on the front panel Jitter Clock Output will also change the level appearing on the pattern generator data output (connected to the Jitter port).
Options	
N4960A-CJ0	Single tone sinusoidal jitter, low (SJ) and high (PJ) deviation, plus external input
N4960A-CJ1	Two internal sinusoidal jitter, true random (RJ) jitter, plus external input
SJ frequency range	With no pattern generator head connected to Jitter port: 1 Hz to 200 MHz With an N4951A/B pattern generator head connected to the Jitter port: 1 Hz to 150 MHz, over-programmable to 200 MHz
SJ modulation range	Range of SJ1 and SJ2. The maximum combined peak jitter of SJ1 + SJ2 + RJ (p-p) + external jitter are applied to the high frequency band modulator (see Figures 25 and 26)
With no pattern generator head connected to the Jitter port:	
Front panel output frequency 1 GHz to 3 GHz	0 to 1.0 UI p-p for modulation frequency 1 Hz to 100 MHz, 0 to 0.5 UI p-p for modulation frequency > 100 MHz to 200 MHz, over-programmable to 1.0 UI
Front panel output frequency > 3 GHz to 16 GHz	0 to 1.0 UI p-p for modulation frequency 1 Hz to 100 MHz, 0 to 0.7 UI p-p for modulation frequency > 100 MHz to 200 MHz, over-programmable to 1.0 UI
With an N4951A/B pattern generator head connected to the Jitter port:	
Front panel output frequency > 2 GHz to 16 GHz	0 to 0.4 UI p-p for modulation frequency 1 Hz to 30 MHz, 4 to 32 Gb/s 0 to 0.165 UI p-p for modulation frequency >30 MHz to 150 MHz, 4 to 29 Gb/s 0 to 0.1 UI p-p for modulation frequency >30 MHz to 150 MHz, >29 to 31.5 Gb/s over-programmable to 0.5 UI
RJ modulation frequency contour	Flat from DC to modulator band pass: –3 dB @ 320 MHz, single pole roll off to 500 MHz. Loop through allows user to customize contour by inserting HPF or LPF in loop on rear panel. Nominal impedance is 50 Ω. Filter insertion loss will lower RJ modulation depth below calibrated value
RJ modulation range	
With no pattern generator head connected to the Jitter port:	
	0 to 25 mUI rms, can be set up to 150 mUI rms, to allow for insertion loss in external filters, but is uncalibrated for settings > 25 mUI. Peak sum of all SJ, RJ and External input applied to high frequency modulation input is limited. Refer to SJ modulation range specification or Figures 25 or 26.
With an N4951A/B pattern generator head connected to the Jitter port:	
	0 to 12 mUI rms, 4 to 29 Gb/s 0 to 7 mUI rms, >29 to 31.5 Gb/s Over-programmable to 25 mUI
RJ crest factor	14 minimum (p-p to rms ratio)

External high frequency band input	
Configuration	Wide band low deviation external modulation input. External input is summed with SJ1, SJ2, and RJ. High frequency band stress is not available when either low frequency PJ or external is selected.
Modulation frequency range	DC to at least 350 MHz, determined by high frequency modulator. –3 dB BW » 320 MHz
Modulation Range	peak sum of all SJ, RJ and external input applied to high frequency modulation input is limited. Refer to SJ modulation range specification or Figures 25 and 26.
Low frequency (high deviation) modulation configuration	Periodic jitter (PJ) or external input. SJ, RJ and high frequency external modulation sources are not available when either low frequency source is enabled.
Low frequency modulation frequency range	
PJ	1 Hz to 17 MHz
External	1 Hz to 4 MHz
Low frequency PJ modulation range	
With no pattern generator head connected to the Jitter port: Front panel output frequency 1 to 16 GHz	0.001 to 100 UI for frequency ≤ 62.5 kHz 0.001 to (6.25E6/ PJ frequency) for frequency > 62.5 kHz to 17 MHz (see Figure 25)
With an N4951A/B pattern generator head connected to the Jitter port: Front panel output frequency > 2 GHz to 16 GHz	0.001 to 50 UI for frequency ≤ 62.5 kHz 0.001 to (3.125E6/ PJ frequency) for frequency > 62.5 kHz to 17 MHz (see Figures 25 and 26)
Low frequency external modulation range	
With no pattern generator head connected to the Jitter port: Front panel output frequency 1 to 16 GHz	0.001 to 50 UI for frequency ≤ 68.4 kHz 0.001 to (3.42E6/modulation frequency) for frequency > 68.4 kHz to 4 MHz (see Figure 25)
With an N4951A/B pattern generator head connected to the Jitter port: : Front panel output frequency > 2 GHz to 16 GHz	0.001 to 25 UI for frequency ≤68.4 kHz 0.001 to (1.71E6/modulation frequency) for frequency > 68.4 kHz to 4 MHz (see Figure 25 and 26)

Maximum N4960A CLOCK OUTPUT modulation range when no pattern generator remote head is connected
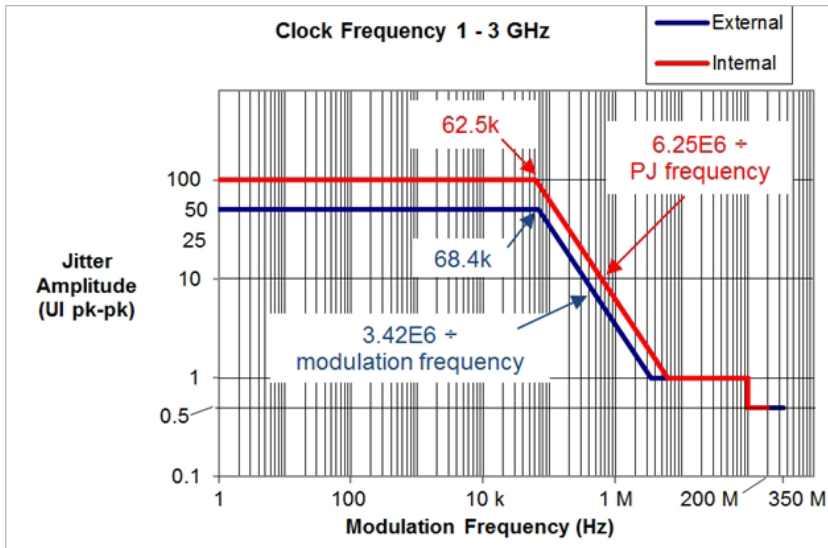

Figure 25a. Clock frequency 1 to 3 GHz; Maximum N4960A JITTER CLOCK OUTPUT modulation amplitude when no remote pattern generator head is attached to the Jitter port..

Figure 25b. Clock frequency > 3 to 15 GHz; Maximum N4960A JITTER CLOCK OUTPUT modulation amplitude when no remote pattern generator head is attached to the Jitter port..
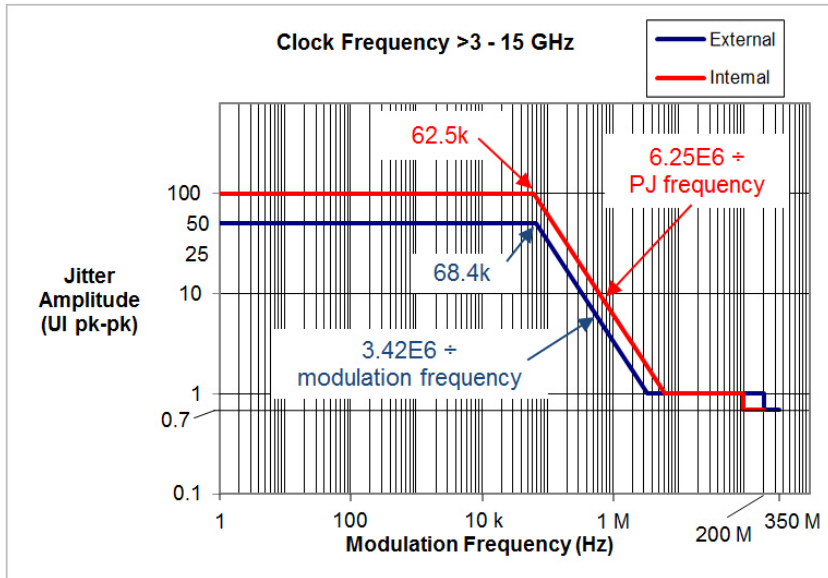

Figure 25c. Clock frequency > 15 to 16 GHz; Maximum N4960A JITTER CLOCK OUTPUT modulation amplitude when no remote pattern generator head is attached to the Jitter port..

Maximum N4960A CLOCK OUTPUT and N4951A/B DATA OUTPUT modulation ranges when a pattern generator remote head is connected

Figure 26a. Maximum N4960A JITTER CLOCK OUTPUT modulation amplitude when a remote pattern generator head is attached to the Jitter port.
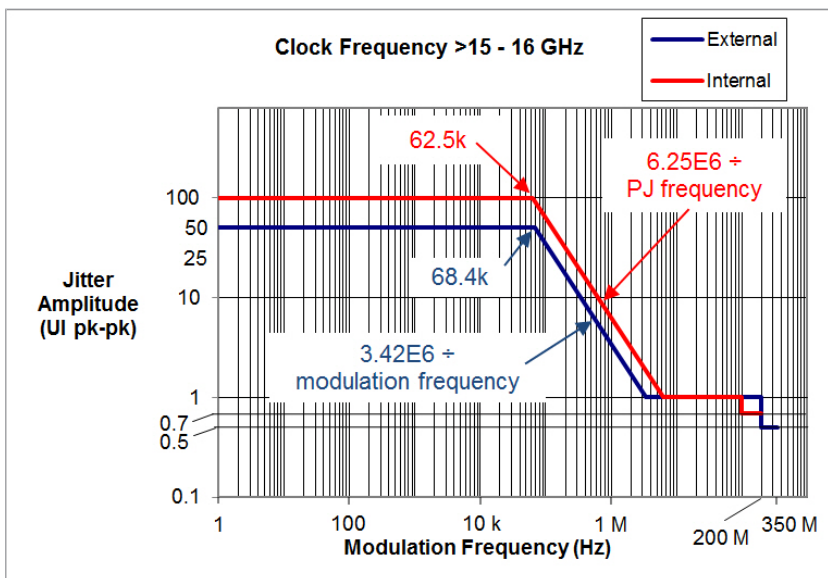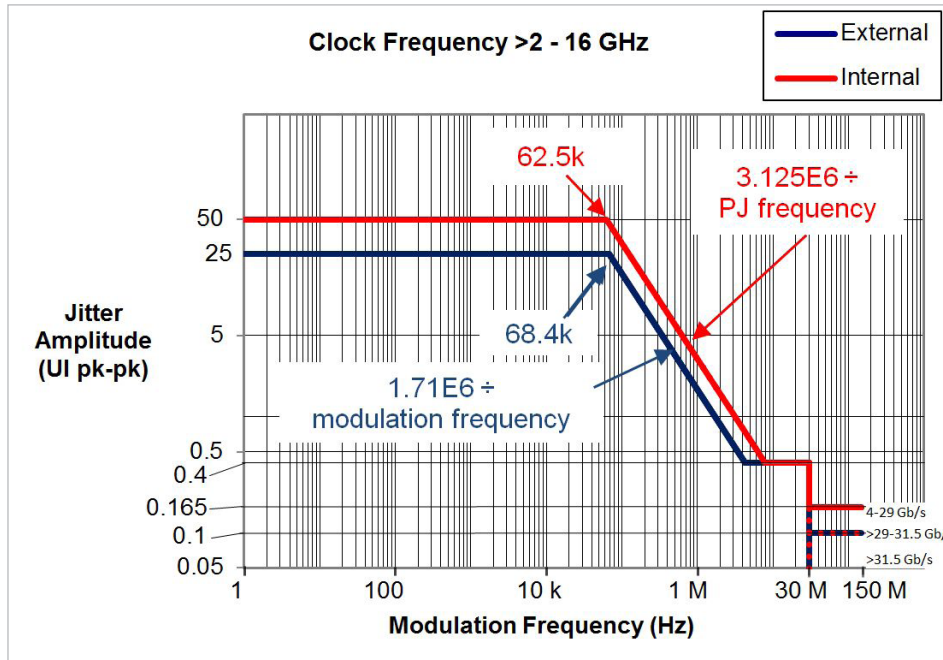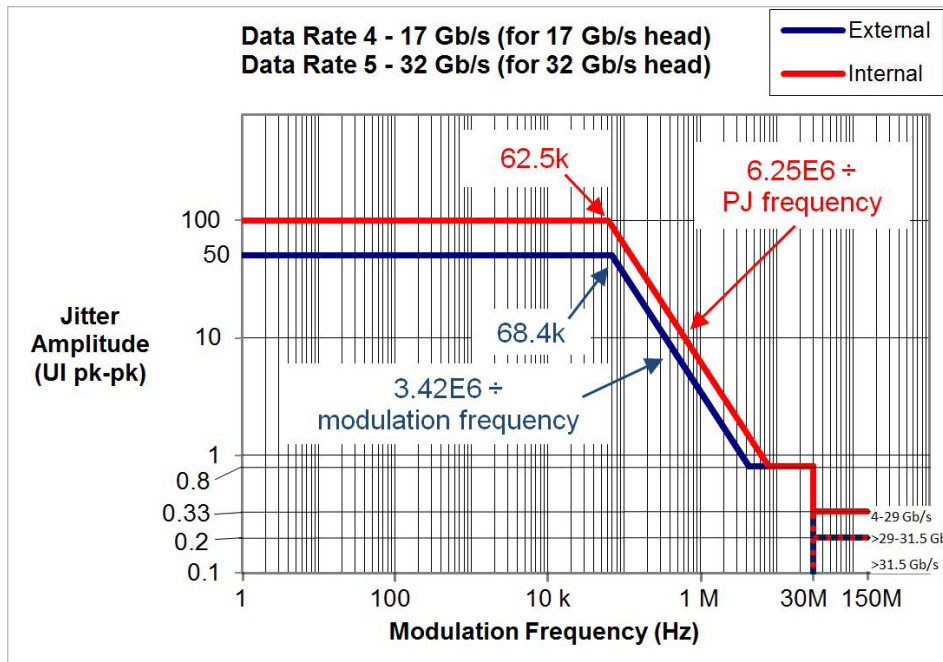

Figures 26b. Maximum N4951A/B Pattern Generator Remote Head DATA OUTPUT modulation amplitude.

N4951A/N4951B[7] pattern generator remote head specifications

Configuration	Remote mountable head operates with N4960-CJ0 / N4960A-CJ1.
Data rate range N4951A-P32/N4951B-H32 / N4951B-D32	5 to 32 Gb/s
Data rate range N4951A-P17/N4951B-H17 / N4951B-D17	4 to 17 Gb/s
Data rate resolution	2 kb/s
Pattern selection	
PRBS (hardware generated)	$2^n - 1$, n = 7, 9, 10, 11, 15, 23, 29, 31, 33, 35, 39, 41, 45, 47, 49, 51
Telecom/datacom	K28.3, K28.5, K28.7, CJPAT, CJTPAT, CRPAT, JSPAT, JTSPAT
Clock	÷ 2, ÷ 4, ÷ 8, ..., ÷ 64, ÷ 2 = 0101, ÷ 4 = 0011, ..., ÷ 64 = 32 0's followed by 32 1's
User	1 bit to 8 Mb
Pattern invert	Available for all patterns
Error injection	Single or uniform rate
Error injection rates	10^{-n}, n = 3, 4, 5, 6, 7, 8, 9
Output configuration	Differential. May be operated single-ended without unused output terminated into 50 Ω. AC Coupled with internal bias tee
Output data connectors	
N4951A	2.92 mm female
N4951B	2.4 mm female
Output data amplitude	
N4951A	100 mV (p-p) to 1.0 V (p-p), single-ended, in 5 mV steps
N4951B-H17/N4951B-H32	300 mV (p-p) to 3.0 V (p-p), single-ended, in 5 mV steps
N4951B-D17/D32	300 mV (p-p) to 1.5 V (p-p), single-ended, in 5 mV steps
Output data crossing point	Adjustable 35 to 65%
Offset voltage range	–2 V to +2 V. Offset range limited by termination voltage
Termination voltage range	–2 V to +2 V. Termination voltage limited by offset voltage
Output data delay range	0 to ±2,000 UI[6], in 2 mUI steps
Rise time (20% to 80%)	
N4951A-P17	17 ps typical, 20 ps maximum[1, 3]
N4951A-P32	16 ps typical, 20 ps maximum[2, 3]
N4951B-H17	12 ps typical, 15 ps maximum[1, 4]
N4951B-H32	12 ps typical. 15 ps maximum[2, 4]
N4951B-D17	16 ps typical, 20 ps maximum[1]
N4951B-D32	15 ps typical, 19 ps maximum[2]
Jitter[6]	
N4951A	1.3 ps rms typical[5]
N4951B-H17	< 750 fs typical[1, 4, 5]
N4951B-H32	< 650 fs typical[2, 4, 5]
N4951B-D17	< 600 fs typical[1,5]
N4951B-D32	< 650 fs typical[2,5]
De-emphasis configuration	5-tap: pre-cursor, post-cursor 1, post-cursor 2, post-cursor 3
N4951B-D17	Pre-cursor 0 to +30 dB[8]
N4951B-D32 only	Post-cursor 1 0 to –30 dB[8]
	Post-cursor 2 –30 to +30 dB[8]
	Post-cursor 3 –30 to +30 dB[8]

1. At 14 Gb/s
2. At 28 Gb/s
3. At 1 V (p-p) amplitude, single-ended
4. At >= 1 V (p-p) amplitude, single-ended
5. Jitter rms is measured on an eye diagram from 86100 DCA with 70 GHz remote heads and precision time base, N4960A driven with an external clock e.g. Keysight E8257D
6. Data Delay spec applies only to a pattern generator connected to the Delay port.
7. N4951B pattern generator heads are only supported on Keysight N4960A controllers with serial numbers higher than US53083001, otherwise an N4960A controller upgrade is required.
8. Cursor amplitudes are specified relative to the preceding cursor e.g. post-cursor 1 amplitude is relative to the main cursor amplitude; post-cursor 2 amplitude is relative to post-cursor 1; post-cursor 3 amplitude is relative to post-cursor 2; pre-cursor amplitude is relative to post-cursor 3.

N4951A/N4951B[7] pattern generator remote head specifications (cont'd)

SJ[1] frequency range	1 Hz to 150 MHz, over-programmable to 200 MHz
SJ modulation range	Range of SJ1 and SJ2. The maximum combined peak jitter of SJ1 + SJ2 +RJ (p-p) + external jitter are applied to the high frequency band modulator (see Figure 26).
	0 to 0.8 UI p-p for modulation frequency 1 Hz to 30 MHz, 4 to 32 Gb/s
	0 to 0.33 UI p-p for modulation frequency >30 MHz to 150 MHz, 4 to 29 Gb/s
	0 to 0.2 UI p-p for modulation frequency >30 MHz to 150 MHz, >29 to 31.5 Gb/s
	Over-programmable to 1.0 UI
RJ[1] modulation range	0 to 24 mUI rms, 4 to 29 Gb/s
	0 to 14 mUI rms, >29 to 31.5 Gb/s
	Over-programmable to 50 mUI rms
Low frequency PJ[1] modulation range	0.002 to 100 UI for frequency ≤ 62.5 kHz
	0.002 to (6.25E6/ PJ frequency) for frequency > 62.5 kHz to 17 MHz (see Figure 26)
Low frequency external modulation range	0.001 to 50 UI for frequency ≤ 68.4 kHz
	0.001 to (3.42E6/modulation frequency) for frequency > 68.4 kHz to 4 MHz (see Figure 26)
High frequency external modulation range	See Figure 20
Indicators	Ch ID – connected to N4960A channel
	Atten – error condition occurred and logged in error log
	On – data output on

1. Jitter injection specs (SJ, PJ, RJ, Ext) apply only to a pattern generator connected to the Jitter port.

N4952A-E32/-E17 error detector remote head specifications

Configuration	Remote mountable head operates with N4960A-CJ0/N4960A-CJ1.
Data rate range (N4952A-E32)	5 to 32 Gb/s
Data rate range (N4952A-E17)	4 to 17 Gb/s
Data rate resolution	2 kb/s
Pattern selection	
PRBS (hardware generated)	$2n - 1$, n = 7, 9, 10, 11, 15, 23, 29, 31, 33, 35, 39, 41, 45, 47, 49, 51
Telecom/datacom	K28.3, K28.5, K28.7, CJPAT, CJTPAT, CRPAT, JSPAT, JTSPAT
Clock	÷ 2, ÷ 4, ÷ 8, ..., ÷ 64. ÷ 2 = 0101, ÷ 4 = 0011 ,..., ÷ 64 = 32 0's followed by 32 1's
User	1 bit to 8 Mb
Input configuration	Differential. May be single-ended with unused input terminated into 50 Ω (termination included), AC coupled with internal bias tee
Input connectors	2.92 mm female
Maximum input amplitude	1 V (p-p) single-ended; 2 V (p-p) differential
Input sensitivity	< 85 mV (p-p) single-ended[1] (typically <50 mV)
Termination voltage	–2 V to +2 V
Input data delay range	0 to ±2,000 UI in 2 mUI steps
Input data decision threshold range	–1 V to + 1 V in 1 mV steps
Indicators	Ch ID – connected to N4960A channel
	Run – BER measurement running
	Errors – bit errors occurring
	Data loss – no data detected
	Sync loss – not synchronized to the incoming data stream
	Atten – error condition occurred and recorded into error log

1.   At <= 28 Gb/s

General specifications

Remote Control Interface	USB2.0 and IEEE-488 (GPIB)
Power Requirements	
Voltage	100 to 240 VAC, auto-ranging
Frequency	50 to 60 Hz
Power Consumption	170 W maximum
Temperature, Operating	+15º to +35º C
Temperature, Non-Operating	–40º to +70º C
Dimensions (Height, Width, and Depth)	
N4960A	100 mm (3.9 in) x 214 mm (8.4 in) x 425 mm (16.7 in)
N4951A	50 mm (1.9 in) x 109 mm (4.3 in) x 222 mm (8.7 in)
N4952A	50 mm (1.9 in) x 109 mm (4.3 in) x 222 mm (8.7 in)
N4951B	50 mm (1.9 in) x 109 mm (4.3 in) x 273 mm (10.75 in)
PG/ED Cable Length	1.0 m (39.7 in)
Mass	
N4960A	3.2 kg (7.0 lbs)
N4951A (with cable)	0.86 kg (30.3 oz)
N4952A (with cable)	0.86 kg (30.3 oz)
N4951B (with cable)	1.0 kg (35.3 oz)

Regulatory standards

EMC	
Complies with European EMC Directive 2004/108/EC	– IEC/EN 61326-1 – CISPR Pub 11 Group 1, class A – AS/NZS CISPR 11 – ICES/NMB-001
	This ISM device complies with Canadian ICES-001. Cet appareil ISM est conforme a la norme NMB-001 du Canada.
Safety	
Complies with European Low Voltage Directive 2006/95/EC	– IEC/EN 61010-1, 2nd Edition – Canada: CSA C22.2 No. 61010-1 – USA: UL std no. 61010-1, 2nd Edition
German acoustic statement	
Acoustic noise emission	Geraeuschemission
LpA < 70 dB	LpA < 70 dB
Operator position	Am Arbeitsplatz
Normal position	Normaler Betrieb
Per ISO 7779	Nach DIN 45635 t.19

Ordering information

All accessories required for operation are shipped with the system including those listed in the accessories tables below and do not need to be purchased separately.

N4960A Accessories

Part number	Qty	Description
12260-002	1	Fuse, 2 A 250 V 5x20 mm, ceramic
12310-025	1	Loop-back cable (opt CJ1 only, installed in rear panel)

N4951A Accessories

Part number	Qty	Description
1810-0118	1	50 ohm termination, SMA
N4960-60018	2	Cable, 2.92 mm M-M, 5.5 in
N4960-60026	2	Cable, 2.92 mm M-F, 5.5 in
N4960-60023	1	Cable, combo-D, 1 meter (connects controller to remote head)

N4951B Accessories

Part number	Qty	Description
08490-60012	2	10 dB attenuator, 2.4 mm (opt H17, H32 only)
11904-60004	2	Adapter, 2.4 mm F-2.92 mm M
85138-60002	1	50 ohm termination, 2.4 mm
N4960-60006	2	Cable, 1.85 mm M-M, 5.5 in
N4960-60023	1	Cable, combo-D, 1 meter (connects controller to remote head)

N4952A Accessories

Part number	Qty	Description
1810-0118	1	50 ohm termination, SMA
N4960-60018	2	Cable, 2.92 mm M-M, 5.5 in
N4960-60026	2	Cable, 2.92 mm M-F, 5.5 in
N4960-60023	1	Cable, combo-D, 1 meter (connects controller to remote head)
M8000-68750	1	Cable discharger

Ordering information (continued)

Serial BERT 32 Gb/s

Model number	Description
N4960A-CJ0 serial BERT controller	Serial BERT controller
N4960A-CJ1 serial BERT controller with jitter injection	Serial BERT controller with multi-tone jitter injection
N4951A-P32	5 to 32 Gb/s pattern generator remote head
N4951B-H32	5 to 32 Gb/s pattern generator high amplitude remote head
N4951B-D32	5 to 32 Gb/s pattern generator with 5-tap de-emphasis remote head
N4952A-E32	5 to 32 Gb/s error detector remote head

Serial BERT 17 Gb/s

Model number	Description
N4960A-CJ0 serial BERT controller	Serial BERT controller
N4960A-CJ1 serial BERT controller with jitter injection	Serial BERT controller with multi-tone jitter
N4951A-P17	4 to 17 Gb/s pattern generator remote head
N4951B-H17	4 to 17 Gb/s pattern generator high amplitude remote head
N4951B-D17	4 to 17 Gb/s pattern generator with 5-tap de-emphasis remote head
N4952A-E17	4 to 17 Gb/s error detector remote head

Model number	Description
N4980A	Multi-instrument BERT software
N4980A-JTS	Jitter tolerance software package
N4980A-TDS	**De-emphasis tap weight calculator tool (included with N4951B-D17/D32 purchase)**

Warranty and calibration service

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