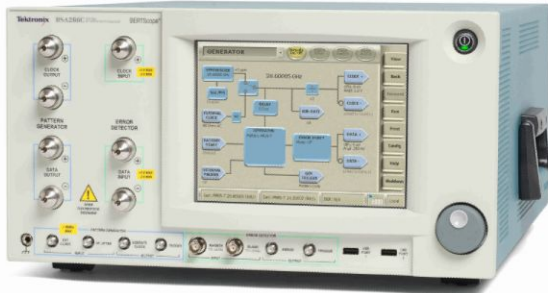# Bit Error Rate Tester

BERTScope® BSA Series Datasheet

The BERTScope Bit Error Rate Tester Series provides a new approach to signal integrity measurements of serial data systems. Perform bit error rate detection more quickly, accurately, and thoroughly by bridging eye diagram analysis with BER pattern generation. The BERTScope Bit Error Rate Tester Series enable you to easily isolate problematic bit and pattern sequences, then analyze further with advanced error analysis that deliver unprecedented statistical measurement depth.

Key performance specifications

- Pattern Generation and Error Analysis, High-speed BER Measurements up to 28.6 Gb/s

- Fast Input Rise Time / High Input Bandwidth Error Detector for Accurate Signal Integrity Analysis

- Physical Layer Test Suite with Mask Testing, Jitter Peak, BER Contour, and Q-factor Analysis for Comprehensive Testing with Standard or User-defined Libraries of Jitter Tolerance Templates

- Integrated Eye Diagram Analysis with BER Correlation

- Optional Jitter Map Comprehensive Jitter Decomposition - with Long Pattern (i.e. PRBS-31) Jitter

- Patented Error Location Analysis™ enables Rapid Understanding of your BER Performance Limitations and Assess Deterministic versus Random Errors, Perform Detailed Pattern-dependent Error Analysis, Perform Error Burst Analysis, or Error-free Interval Analysis
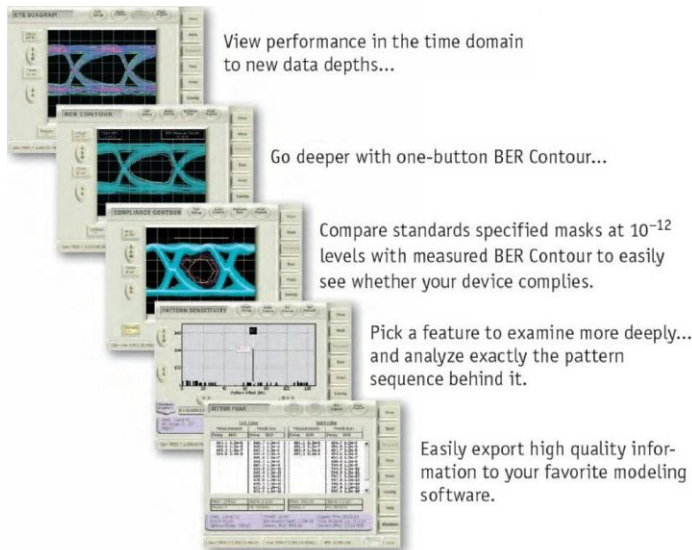
Key features

- Integrated, calibrated stress generation to address the stressed receiver sensitivity and clock recovery jitter tolerance test requirements for a wide range of standards

  - Sinusoidal jitter to 100 MHz
  - Random jitter
  - Bounded, uncorrelated jitter
  - Sinusoidal interference
  - Spread spectrum clocking
  - PCIe 2.0 & 3.0 receiver testing
  - F/2 jitter generation for 8xFC and 10GBASE-KR testing
  - IEEE802.3ba & 32G fibre channel testing

- Electrical stressed eye testing for

  - PCI express
  - 10/40/100 Gb Ethernet
  - SFP+/SFI
  - OIF/CEI
  - Fibre channel (FC8, FC16, FC32)
  - SATA
  - USB 3.1
  - InfiniBand (SDR, QDR, FDR, EDR)

- Tolerance compliance template testing with margin testing

- Integrated eye diagram analysis with BER correlation

Applications

- Design verification including signal integrity, jitter, and timing analysis

- Design characterization for high-speed, sophisticated designs

- Certification testing of serial data streams and high performance Networking systems

- Design/Verification of high-speed I/O components and systems

- Signal integrity analysis – mask testing, jitter peak, BER contour, jitter map, and q-factor analysis

- Design/Verification of optical transceivers

Linking domains

Eye diagrams have always provided an easy and intuitive view of digital performance. It has been harder to tie this directly with BER performance, as the instruments that provide views of each have been architected in fundamentally different ways. Eye diagrams have been composed of shallow amounts of data that have not easily uncovered rarer events. BERTs have counted every bit and so have provided measurements based on vastly deeper data sets, but have lacked the intuitive presentation of information to aid troubleshooting.

View performance in the time domain to new data depths...

Go deeper with one-button BER Contour...

Compare standards specified masks at 10^{-12} levels with measured BER Contour to easily see whether your device complies.

Pick a feature to examine more deeply... and analyze exactly the pattern sequence behind it.

Easily export high quality information to your favorite modeling software.

The BERTScope removes this gap allowing you to quickly and easily view an eye diagram based on at least two orders of magnitude more data than conventional eyes. Seeing a feature that looks out of the ordinary, you are able to place cursors on the item of interest and by simply moving the sampling point of the BERT, use the powerful error analysis capabilities to gain more insight into the feature of interest. For example, check for pattern sensitivity of the latest rising edges. Alternatively, use one-button measurement of BER Contour to see whether performance issues are bounded or likely to cause critical failures in the field. In each case, information is readily available to enhance modeling or aid troubleshooting, and is available for patterns up to $2^{31} - 1$ PRBS.
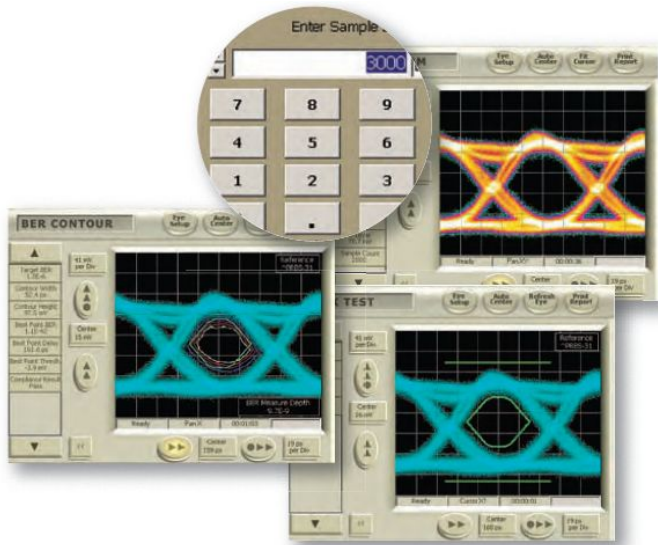
Data rich eye diagrams

As shown previously, there is an impressive difference in data depth between conventional eye diagrams and those taken with a BERTScope. So what does that mean? It means that you see more of what is really going on - more of the world of low-probability events that is present every time you run a long pattern through a dispersive system of any kind, have random noise or random jitter from a VCO - a world that is waiting to catch you out when your design is deployed. Adding to this the deeper knowledge that comes from the one-button measurements of BER Contour, Jitter Peak, and Q-factor, and you can be confident that you are seeing the complete picture.
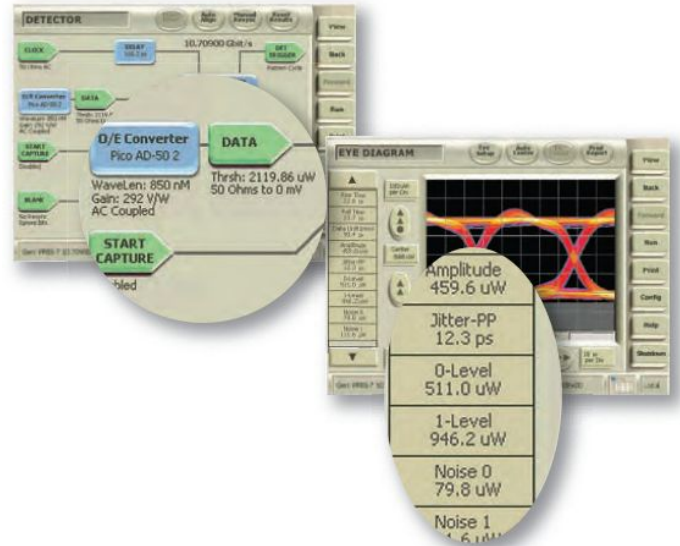
The BERTScope shown with optical units enabled. In this example measurements are converted to the optical domain automatically.

Deep mask testing

With the ability to vary sample depth, it is very easy to move between deep measurements which give a more accurate view of the real system performance, and shallow measurements that match those of a sampling oscilloscope. The measurements shown below are from the eye diagram of an optical transmitter. With the BERTScope sample depth set to only 3000 waveforms, the BERTScope generates the diagram shown in the middle in only 1 second. The measured mask margin of 20% exactly correlates to the same measurement made on a sampling oscilloscope. The lower diagram shows the eye produced by the same device, using Compliance Contour measured at a BER of 1×10^{-6}. Here the mask margin is reduced to 17%.

The depth advantage gained for eye diagrams is at least 10 times greater for mask testing. Unlike pseudo-mask testing offered by some BERTs, a BERTScope mask test samples every point on the perimeter of an industry-standard mask, including the regions above and below the eye. Not only that, but each point is tested to a depth unseen before. This means that even for a test lasting a few seconds using a mask from the library of standard masks or from a mask you have created yourself, you can be sure that your device has no lurking problems.

Accurate jitter testing to industry standards

Testing with long or short patterns, the most accurate jitter measurement is likely to come from the methodology that uses little or no extrapolation to get its result. With the BERTScope, you can quickly measure to levels of 1×10^{-9} (1×10^{-10} at high data rates), or wait for the instrument to measure 1×10^{-12} directly. Either way, the BERTScope's one-button measurements are compliant to the MJSQ jitter methodology, and because the underlying delay control is the best available on any BERT you can be sure that the measurements are accurate. Use the built-in calculations for Total Jitter (TJ), Random Jitter (RJ), and Deterministic Jitter (DJ), or easily export the data and use your own favorite jitter model.

The BSA286CL's low intrinsic RJ supports serving of 802.3ba's simultaneous VECP (Vertical Eye Closure Penalty) and J2/J9 calibration with valuable margin required to fully characterize 100G Ethernet silicon.

Mask compliance contour testing

Many standards such as XFP/XFI and OIF CEI now specify mask tests intended to assure a specified 1×10^{-12} eye opening. Compliance Contour view makes this easy by taking a mask, and overlaying it on your measured BER contours - so you can immediately see whether you have passed the mask at whatever BER level you decide.

Quick selection guide

Model	Maximum bit rate	Stressed eye - SJ, RJ, BUJ, SI
BSA286CL	28.6 Gb/s	Opt. STR
BSA175C	17.5 Gb/s	Opt. STR
BSA125C	12.5 Gb/s	Opt. STR
BSA85C	8.5 Gb/s	Opt. STR

Flexible clocking

The generator clock path features in the BERTScope provides the test flexibility needed for emerging real-world devices. Whether computer cards or disk drives, it is often necessary to be able to provide a sub-rate system clock, such as 100 MHz for PCI Express® (PCIe). To get the target card running may require a differential clock signal with a particular amplitude and offset; this is easily accomplished with the BERTScope architecture, with many flexible divide ratios available.
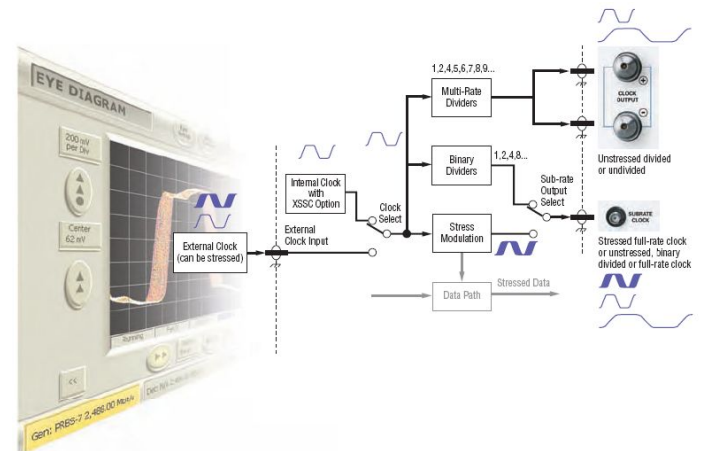
Clock path in BERTScope Option STR models

Spread Spectrum Clocking (SSC) is commonly used in electrical serial data systems to reduce EMI energy by dispersing the power spectrum. Adjustable modulation amplitude, frequency, and a choice of triangle or sine modulation wave shape allow testing receivers to any compliance standard which utilize SSC. An additional modulator and source allows users to stress the clock with high-amplitude, low-frequency Sinusoidal Jitter (SJ).

Working with closed eyes

With the need to push ever-increasing data rates through electrical channels, the frequency-dependent losses often result in eye closure at the receiver end. Engineers use equalization to compensate for these losses and "open the eyes" in the real system. Tektronix offers powerful tools that allow designers to characterize and test compliance of receiver and transmitter components used in these systems.
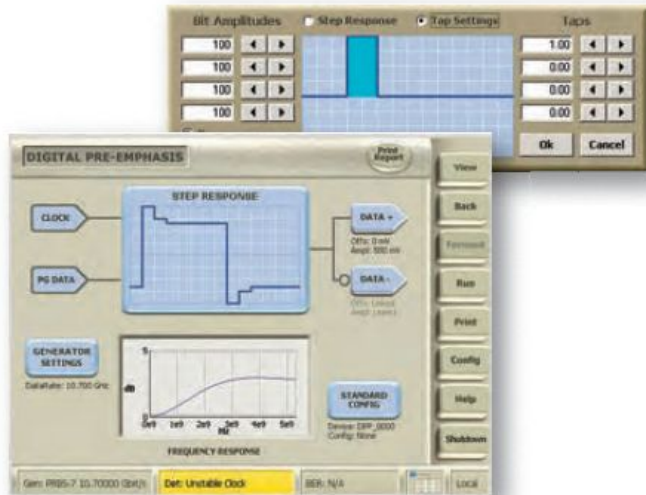
In keeping with the BERTScope philosophy, the graphical user interface presents the control functionality in a logical, easy-to-follow format. A time domain representation of the response shows the effects of tap weight settings. The frequency domain Bode plot shows how the filter will compensate for the channel losses.

For receiver testing, the DPP125C Digital Pre-emphasis Processor adds calibrated pre-emphasis to the BERTScope pattern generator outputs, emulating pre-emphasis applied at the transmitter. Pre-emphasis is currently used in 10GBASE-KR, PCIe, SAS 12 Gb/s, DisplayPort®, USB 3.1, and other standards.

Features:

- 1-12.5 Gb/s clock rates
- 3- or 4-tap versions
- Flexible cursor placement allowing pre-cursor or post-cursor
- Option ECM (Eye opener, Clock Multiplier, Clock Doubler)

PatternVu

The PatternVu option includes a software-implemented FIR filter which can be inserted before the eye pattern display. In systems employing receiver equalization, this allows you to view the eye diagram and perform physical measurements on the eye as the receiver's detector would see it, after the effect of the equalizer. Equalizers with up to 32 taps can be implemented, and the user can select the tap resolution per UI.
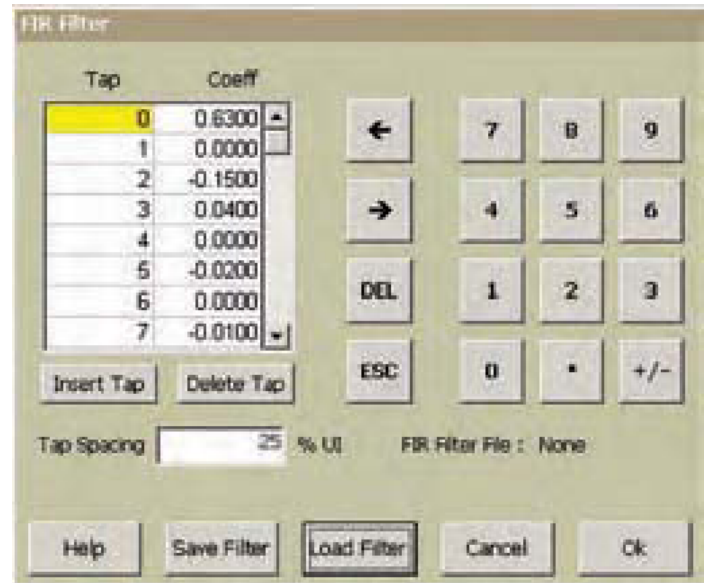
PatternVu

PatternVu also includes CleanEye, a pattern-locked averaging system which removes the nondeterministic jitter components from the eye. This allows you to clearly see pattern-dependent effects such as ISI (Inter-Symbol Interference) which are normally obscured by the presence of high amounts of random jitter.

Single Value Waveform export is a component in the PatternVu option. This allows you to capture a pattern-locked waveform showing single bits, similar to a single-shot capture in a real-time oscilloscope. Once captured, the waveform can be exported in a variety of formats for further analysis in an external program.

Add clock recovery

The Tektronix CR125A, CR175A, and CR286A add levels of flexibility in compliant clock recovery. Most standards requiring jitter measurement specify the use of clock recovery, and exactly which loop bandwidth must be used. Using a different or unknown loop bandwidth will almost certainly give you the wrong jitter measurement. The new clock recovery instrument enables easy and accurate measurements to be made to all of the common standards.
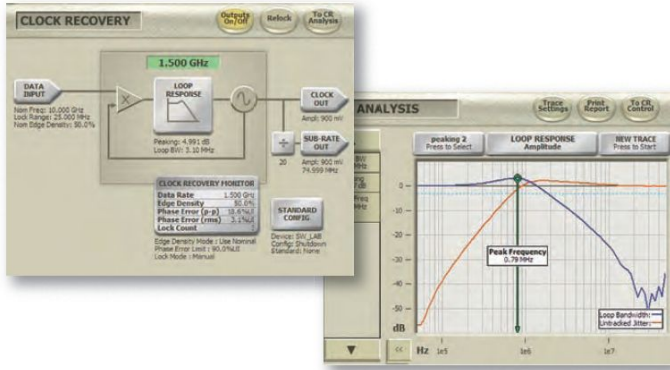
The intuitive user interface provides easy control of all operating parameters. A unique Loop Response view shows the loop characteristics – actually measured, not just the settings value.

The usefulness of the BERTScope CR is not just confined to BERTScope measurements. Use them stand-alone in the lab with your sampling oscilloscopes, or with existing BERT equipment. Compliant measurements are available to you by pairing either of these versatile instruments with your existing investments.
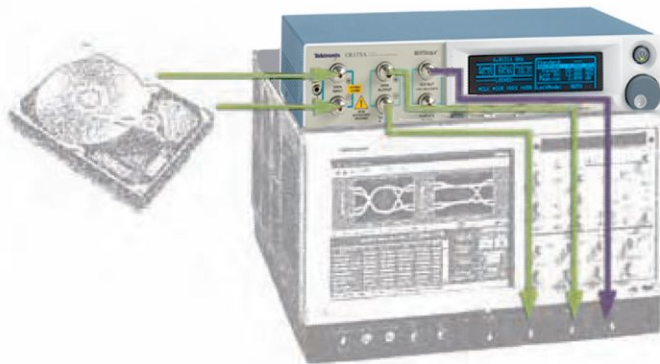
Display and measure SSC modulation

Spread Spectrum Clocking (SSC) is used by many of the latest serial busses including SATA, PCI Express, and next-generation SAS to reduce EMI issues in new board and system designs. The Tektronix CR Family provides spread spectrum clock recovery together with the display and measurement of the SSC modulation waveform. Automated measurements include minimum and maximum frequency deviation (in ppm or ps), modulation rate of change (dF/dT), and modulation frequency. Also included are display of the nominal data frequency and easy-to-use vertical and horizontal cursors.
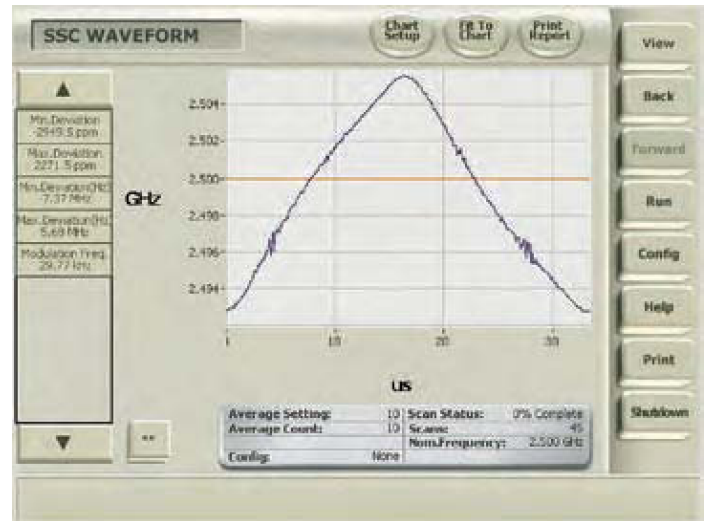
SSC waveform measurement

Add jitter analysis

Combine a Tektronix CR125A, CR175A, or CR286A with Option 12GJ, 17GJ, and 28GJ respectively and your sampling oscilloscope or BERTScope for variable clock recovery from 1.2 to 11.2 Gb/s, Duty Cycle Distortion (DCD) measurement, and real-time jitter spectral analysis. Display jitter spectral components from 200 Hz to 90 MHz with cursor measurements of jitter and frequency. Measure band-limited integrated jitter with user-settable frequency-gated measurements (preset band limits and integrated jitter measurement for PCI Express 2.0 jitter spectrum in this example).
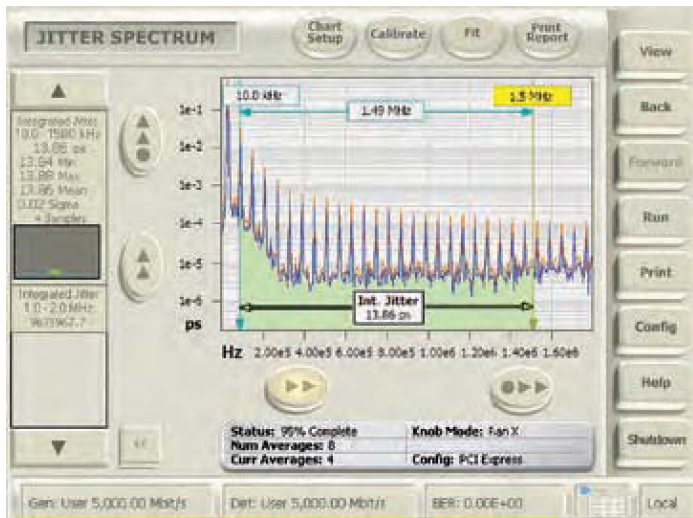
Jitter spectrum measurement

Taking stress out of receiver testing

As networks have changed, so have the challenges of testing receivers. While tests such as BER and receiver sensitivity are still important, receiver jitter tolerance has evolved to be more real-world for jitter-limited systems such as 10 Gb/s data over back planes and new high-speed buses. Stressed Eye testing is becoming increasingly common as a compliance measurement in many standards. In addition, engineers are using it to explore the limits of their receiver performance to check margins in design and manufacturing.

Creating the stress recipe for receiver testing to a complicated standard such as PCIe 2.0 used to require "racking and stacking" several instruments, then spending hours calibrating the setup. With BERTScope, an easy-to-understand graphical view gives you control of all of the calibrated stress sources you need – inside the same instrument. Eliminating the need for external cabling, mixers, couplers, modulators, etc. simplifies stress calibration.
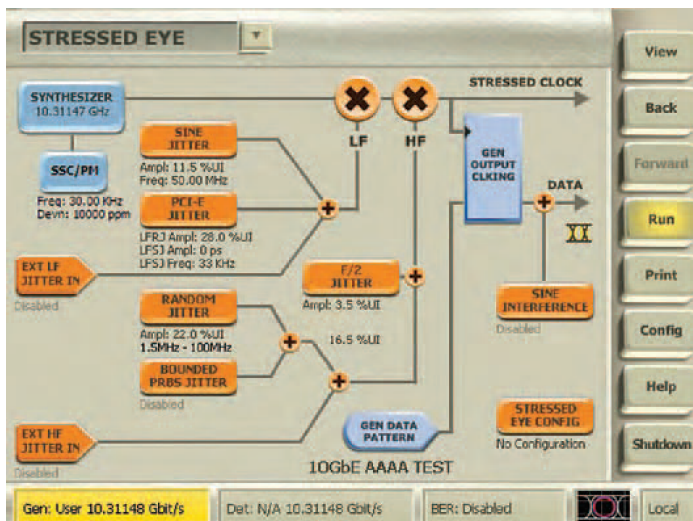
Stressed Eye view

Flexible stress impairments

The BERTScope has high-quality, calibrated sources of stress built-in, including RJ, SJ, BUJ, and SI.

ISI is also a common ingredient in many standards. The BSA12500ISI differential ISI board provides a wide variety of path lengths, free from switching suck-outs and anomalies.
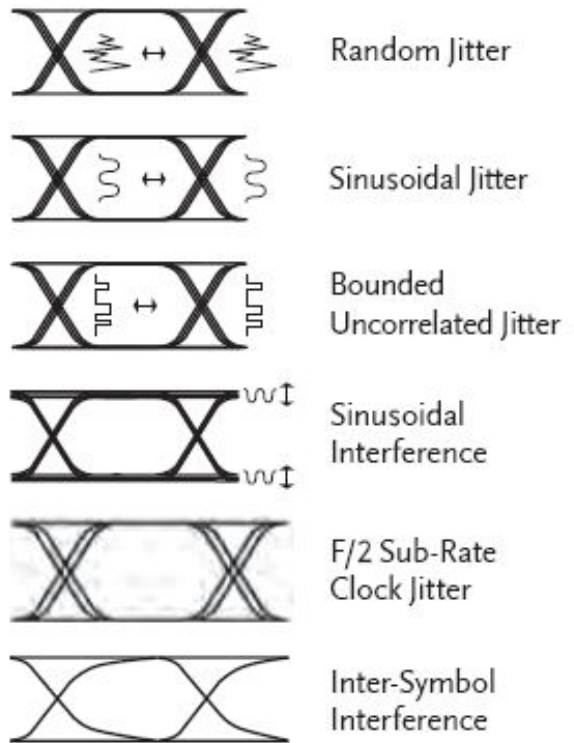
Flexible stress impairments

Many standards call for SJ to be stepped through a template with different SJ amplitudes at particular modulation frequencies. This is easy with the built-in Jitter Tolerance function which automatically steps through a template that you designed, or one of the many standard templates in the library.
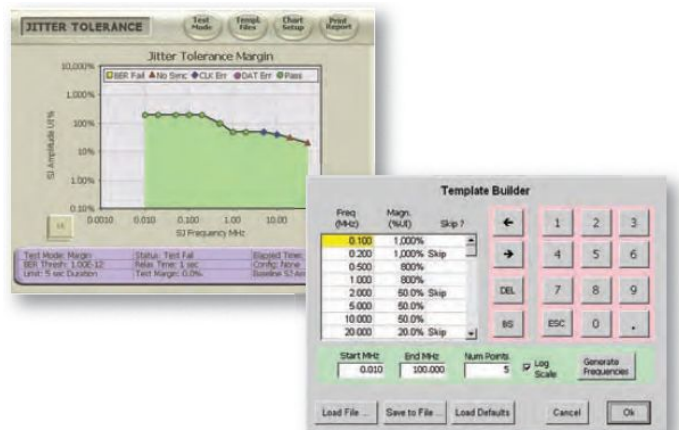
Built-in jitter tolerance function

BERTScope pattern generators

The BERTScope pattern generators provide a full range of PRBS patterns, common standards-based patterns, and user-defined patterns.

Option STR provides full integrated, calibrated stress generation which is an easy-to-use alternative to a rack full of manually calibrated instruments needed to provide a stressed pattern. Uses include receiver testing of devices with internal BER measurement ability such as DisplayPort, or adding stress capability to legacy BERT instruments.
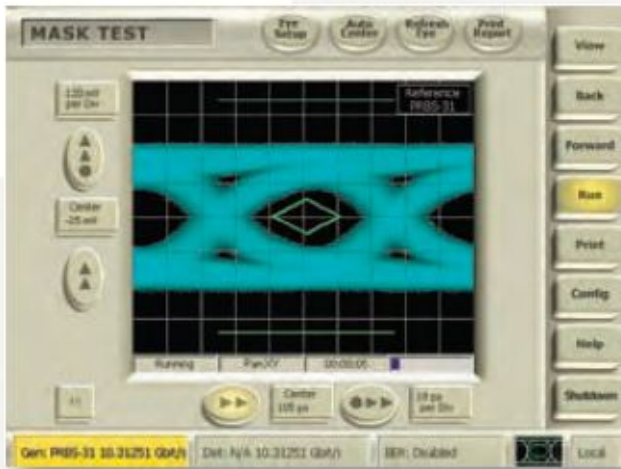

XFI compliant electrical stressed eye

Stressed eye option

Pattern capture

There are several methods for dealing with unknown incoming data. In addition to Live Data Analysis discussed above, a useful standard feature on all BERTScope analyzers is pattern capture. This allows the user to specify the length of a repeating pattern and then allow the analyzer to grab the specified incoming data using the detector's 128 Mb RAM memory. This can then be used as the new detector reference pattern, or edited and saved for later use.
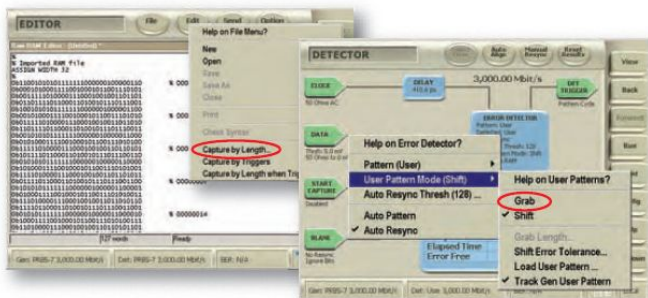
Pattern capture

Using the Power of Error Analysis – In the following example eye diagram views were linked with BER to identify and solve a design issue in a memory chip controller. The eye diagram (top left) shows a feature in the crossing region that is unexpected and appearing less frequently than the main eye. Moving the BER decision point to explore the infrequent events is revealing. Error Analysis shows that the features are related in some way to the number 24. Further investigation traced the anomaly to clock breakthrough within the IC; the system clock was at 1/24th of the output data rate. Redesigning the chip with greater clock path isolation gave the clean waveform of the top right eye diagram.
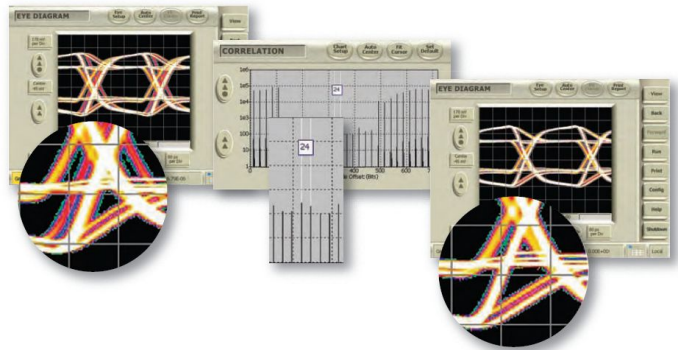
Power of error analysis example

Pattern generator stressed eye

The pattern generator stressed eye function provides the following features:

- Flexible, integrated stressed eye impairment addition to the internal or an external clock

- Easy setup, with complexity hidden from the user with no loss of flexibility

- Verify compliance to multiple standards using the BERTScope and external ISI filters. Standards such as:
  - OIF CEI
  - 6 Gb SATA
  - PCI Express
  - XFI
  - USB 3.1
  - SONET
  - SAS 2
  - XAUI
  - 10 and 100 Gb Ethernet
  - DisplayPort

- Sinusoidal interference may be inserted in-phase or in anti-phase, or sent externally to be summed after an external ISI reference channel

- Sinusoidal jitter may be locked between two BERTScopes in-phase or anti-phase, as required by OIF CEI

Amplitude and ISI impairments

For ISI, add externally: for example, long coaxial cable length, or Bessel-Thompson 4th Order Filter with –3 dB point at 0.75 of bit rate, etc.

For applications requiring circuit board dispersion, the BSA12500ISI differential ISI accessory board can be used.

Sinusoidal interference

- Supports full data rate range of BERTScope

- 100 MHz to 2.5 GHz

- Adjustable in 100 kHz steps

- Adjustable from 0 to 400 mV

- Common mode or differential

- Available from the rear-panel 50 Ω SMA connector, single ended with data amplitude from 0 to 3 V adjustable from GUI, same frequency range and step size as internal adjustment

Jitter measurements

Multi-gigabit serial data channels have eye openings only a couple hundred picoseconds wide – or less. In systems where only a few picoseconds of jitter count, accurate measurement of jitter is essential for managing tight jitter budgets. The BERTScope has two sets of tools which perform these critical measurements.

The Physical Layer Test Suite option includes measurement of Total Jitter (TJ) along with breakdown into Random Jitter (RJ) and Deterministic Jitter (DJ), using the well-accepted Dual Dirac method. The deep, BERT-collected measurements use several orders of magnitude less extrapolation, or in some cases no extrapolation, than oscilloscopes use as a basis for the jitter measurements. This produces inherently more accurate results than measurements made on other instruments which rely on high levels of extrapolation.
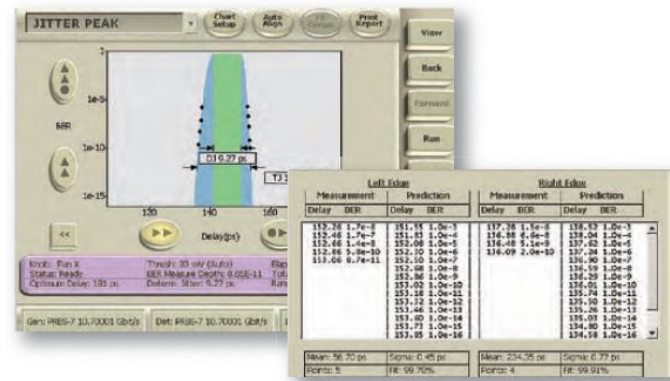
MJSQ-compliant Dual Dirac jitter measurement.

The optional Jitter Map is the latest suite of jitter measurements available for the BERTScope. It provides a comprehensive set of subcomponent analysis beyond RJ and DJ, including many measurements compliant with higher data rate standards. Jitter Map can also measure and decompose jitter on extremely long patterns, such as PRBS-31, as well as live data (requires Live Data Analysis option) providing that it can first run on a shorter synchronized data pattern.
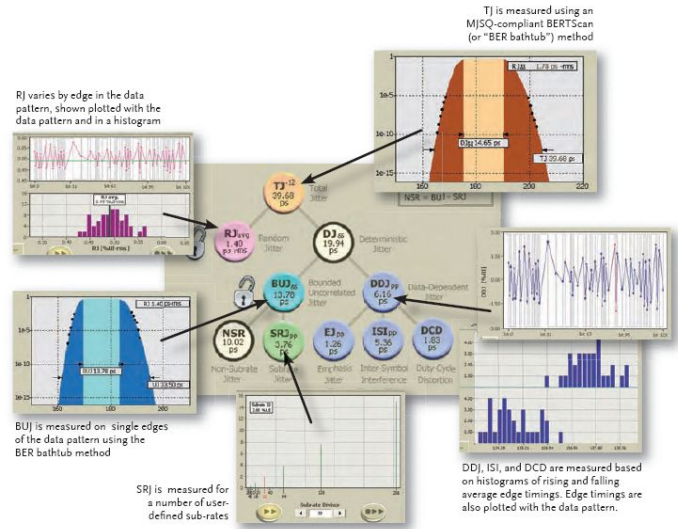
Jitter map

Features include:

- DJ breakdown into Bounded Uncorrelated Jitter (BUJ), Data Dependent Jitter (DDJ), Inter-Symbol Interference (ISI), Duty Cycle Distortion (DCD), and Sub-Rate Jitter (SRJ) including F/2 (or F2) Jitter

- BER-based for direct (non-extrapolated) Total Jitter (TJ) measurement to 10^{-12} BER and beyond

- Separation of correlated and non-correlated jitter components eliminates mistaking long pattern DDJ for RJ

- Can measure jitter with minimum eye opening

- Additional levels of breakdown not available from other instruments such as: Emphasis Jitter (EJ), Uncorrelated Jitter (UJ), Data Dependent Pulse Width Shrinkage (DDPWS), and Non-ISI

- Intuitive, easy-to-navigate jitter tree
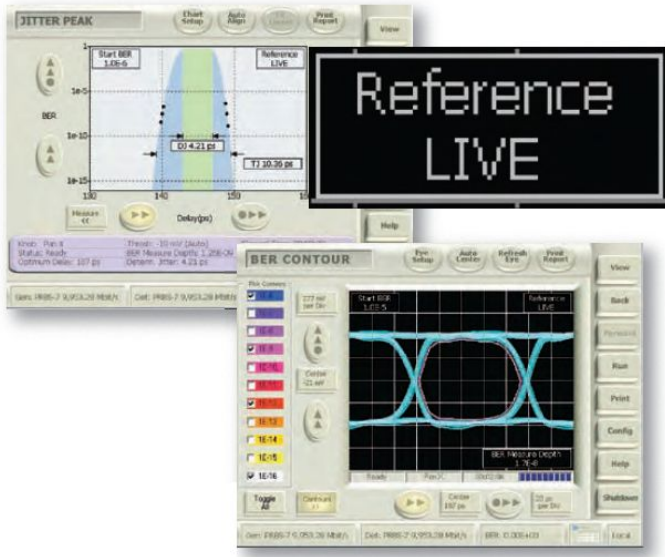
Jitter peak and BER contour measurements made on live data.

Flexible external jitter interfaces

Flexible external jitter interfaces include the following features:

- Front panel external high frequency jitter input connector – jitter from DC to 1.0 GHz up to 0.5 UI (max) can be added, of any type that keeps within amplitude and frequency boundaries

- Rear panel external SJ low frequency jitter input connector – jitter from DC to 100 MHz up to 1 ns (max) can be added

- Rear panel SJ output

- Sinusoidal interference output rear panel connector

The internal RJ, BUJ, and external high-frequency jitter input is limited to 0.5 UI, combined, further limited to 0.25 UI each when both are enabled. Rear-panel low-frequency jitter input can be used to impose additional jitter; the sum of external low-frequency jitter, internal low-frequency SJ to 10 MHz, PCIe LFRJ and PCIe LFSJ (with Option PCISTR) is limited to 1.1 ns. This limit does not apply to Phase Modulation (PM) from Option XSSC.

Jitter impairments

Bounded uncorrelated jitter:

- Supports data rates from 1.5 to 8.5 Gb/s (BSA85C), to 12.5 Gb/s (BSA125C), 17.5 Gb/s (BSA175C), and 28.6 Gb/s (BSA286CL) with limited performance to 622 Mb/s (BSA286CL excluded)

- Internal PRBS Generator

- Variable up to 0.5 UI

- 100 Mb/s to 2.0 Gb/s

- Band-limited by selected filters

BUJ rate	Filter
100 to 499	25 MHz
500 to 999	50 MHz
1,000 to 1,999	100 MHz
2,000	200 MHz

Random jitter:

- Supports data rates from 1.5 to 8.5 Gb/s (BSA85C), to 12.5 Gb/s (BSA125C), 17.5 Gb/s (BSA175C), and 28.6 Gb/s (BSA286CL) with limited performance to 622 Mb/s (BSA286CL excluded)

- Variable up to 0.5 UI

- Band-limited 10 MHz to 1 GHz

- Crest factor of 16 (Gaussian to at least 8 standard deviation or about 1×10^{-16} probability)

Sinusoidal jitter

Data rate	Internal SJ frequency	Maximum internal SJ amplitude
Up to 8.5 Gbps (BSA85C), 12.5 Gbps (BSA125C, or 17.5 Gbps (BSA175C)	1 kHz to 10 MHz [1]	1100 ps
	10 MHz to 100 MHz	200 ps
Up to 28.6 Gb/s (BSA286CL)	1 kHz to 100 MHz	1100 ps [2] 270 ps [3]

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[1] Can be combined with other low-frequency modulation.

[2] Full SJ range is 270 ps with RJ or BUJ the range is reduced to 220 ps.

[3] Range is selectable between 1100 ps and 270 ps maximum; a lower range has lower intrinsic jitter.

SJ adjustable from 0 to levels greater than or equal to range in table. See *Additional stress options* for more SJ capabilities.

BSASWITCH instrument switch

User interfaces

User interfaces take usability to new heights:

- Easy navigation
- Logical layout and operation
- Multiple ways of moving between screens
- Relevant information right where you need it
- Color coding to alert you to the presence of nonstandard conditions
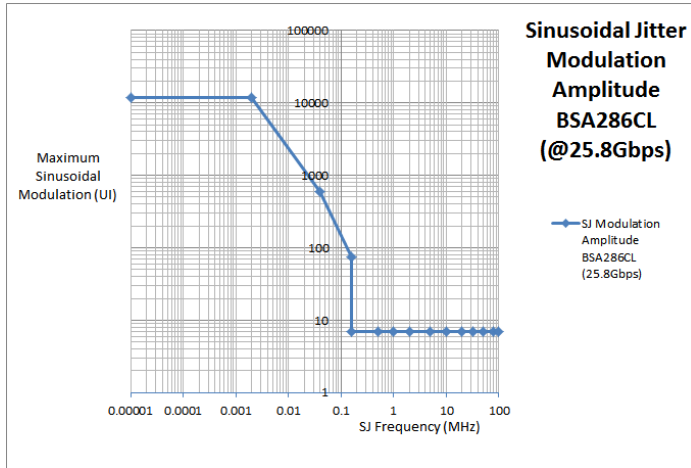
Testing interface cards

Finally a solution to the age-old problem of making physical layer measurements on high-speed line cards, motherboards, and live traffic – the BERTScope Live Data Analysis option. Through novel use of the dual-decision point architecture, the instrument is able to make parametric measurements such as Jitter, BER Contour, and Q-factor in addition to the eye and mask measurements that are usable as standard – all that is required is a clock signal. Add the Jitter Map option to see even more layers of jitter decomposition on live data. No more frustration because the pattern is not known, is unpredictable, or involves rate-matching word insertions. Troubleshooting is so much easier now that the one-button physical layer tests can be employed to provide unique insight.

Using the USB3 instrument switch

The BSASWITCH Instrument Switch is a flexible device usable for general-purpose applications and specific inclusion in USB 3.1 compliance testing. For USB 3.1 testing, the switch features a pattern generator for generation of Low Frequency Periodic Signaling (LFPS), used to ensure devices achieve loopback. Other features include:

- Manual switching between channels with front-panel controls
- Automated control through USB
- Flexible triggering with multiple control choices
- Two main input channels (Ch 1, Ch 2) with >10 GHz analog bandwidth
- Single-ended to differential input channel for easily adding low-frequency signal generators to test setups
- USB control and power with no need for additional external power
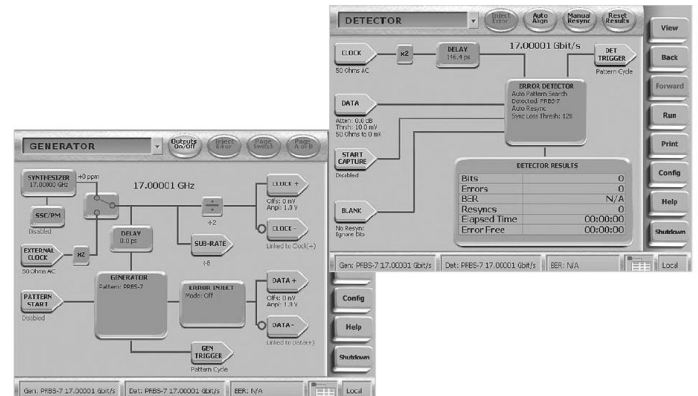
UI setup screens

Use the Editor screen for pattern editing of standard and AB page select patterns and mask editing and other tasks:

- Views in Binary, Decimal, or Hexadecimal
- Support for variable assignments, repeat loops, seeding of PRBS patterns
- Capture and editing of incoming data – for example, to make a repeating pattern out of real-world traffic
  - Capture is available by trigger, by length, or by length following a trigger
  - Capture is by number or words, 1 word is 128 bits. For example, a PRBS-7 (127 bits long) would be captured as 127 words, and would have overall length of 16,256 bits
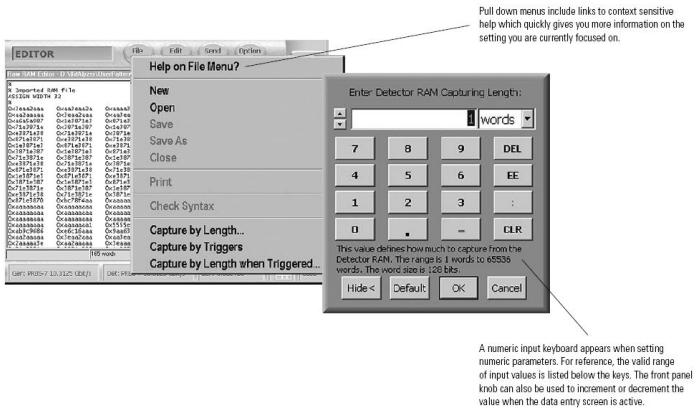
Editor screen

BERTScope built-in parametric measurements

All BERTScopes come with eye diagrams and mask test capabilities as standard, along with error analysis.

Eye diagrams:

- 280×350 pixel waveform display
- Deep acquisition
- Automatic Measurements include:
  - Rise time
  - Fall time
  - Unit interval (data, and also clock)
  - Eye amplitude
  - Noise level of 1 or 0
  - Eye width
  - Eye height
  - Eye jitter (p-p and RMS)
  - 0 level, 1 level
  - Extinction ratio
  - Vertical eye closure penalty (VECP)
  - Dark calibration
  - Signal-to-Noise ratio
  - V_{p-p}, V_{max}, V_{min}, crossing levels
  - Rising and falling crossing level (picoseconds)
  - Overshoot 0 level and 1 level
  - Average voltage/power
  - Cross amplitude, noise level 1 or 0, voltage
  - Optical modulation amplitude (OMA)
  - Sample count
  - Offset voltage
  - De-emphasis ratio

Mask testing:

- Library of standard masks (such as, XFP, or edit custom masks)
- Addition of positive or negative mask margin
- Import of measured BER contour to become process control mask
- At least 1000x the sample depth of traditional sampling oscilloscope masks is ideal for ensuring the absence of rare event phenomena

Optical units:

- An external optical receiver can be added to the input of the BERTScope detector. Through the user interface it is easy to input and save the characteristics of the receiver. Once accomplished, relevant units on physical layer displays are changed to optical power in dBm, μW, or mW. Coupling can be AC or DC, and the software steps the user through dark calibration.
- For electrical signals, attenuation values can be entered to properly scale eye diagrams and measurements when external attenuators are used.

Variable-depth eye and mask testing:

- For eye diagrams and mask testing, the depth of test may be varied in manual mode; the instrument will take the specified number of waveforms then stop. The range is 2,000 to 1,000,000 bits (complete waveforms). Alternatively, the default mode is Continuous, and the eye or mask test increases in depth over time.

Physical layer test option

The following physical layer test options are available:

- BER contour testing
  - Executed with same acquisition circuitry as eye diagram measurements for maximum correlation
  - As-needed delay calibration for accurate points
  - Automatic scaling, one-button measurement
  - Extrapolates contours from measured data, increasing measurement depth with run time and repeatedly updating curve fits
  - Easy export of fitted data in CSV format
  - Contours available from 10^{-6} to 10^{-16} in decade steps

- Basic jitter measurements
  - Testing to T11.2 MJSQ BERTScan methodology (also called 'Bathtub Jitter')
  - Deep measurements for quick and accurate extrapolation of Total Jitter at user-specified level, or direct measurement
  - Separation of Random and Deterministic components, as defined in MJSQ
  - As-needed delay calibration for accurate points
  - Export of points in CSV format
  - Easy one-button measurement
  - User-specified amplitude threshold level, or automatic selection
  - Selectable starting BER to increase accuracy when using long patterns, as defined in MJSQ
- Q-factor measurement
  - One-button measurement of a vertical cross section through the middle of the eye
  - Easy visualization of system noise effects
  - Export of data in CSV format
- Compliance contour
  - Validation of transmitter eye performance to standards such as XFP/XFI and OIF CEI
  - Overlay compliance masks onto measured BER contours and easily see whether devices pass the BER performance level specified

Live data analysis option

The Live data analysis option is designed to measure parametric performance of traffic that is either unknown or non-repeating. This can include traffic with idle bits inserted, such as, in systems with clock rate matching. It is also suitable for probing line cards.

The option uses one of the two front-end decision circuits to decide whether each bit is a one or zero by placing it in the center of the eye. The other is then used to probe the periphery of the eye to judge parametric performance. This method is powerful for physical layer problems, but will not identify logical problems due to protocol issues, where a zero was sent when it was intended to be a one.

Live data measurements can be made using BER Contour, Jitter Peak, Jitter Map, and Q-factor. Eye diagram measurements can be made on live data without the use of this option, providing a synchronous clock is available.

The Live data analysis option requires the Physical layer test option and must be used with a full-rate clock.

PatternVu equalization processing option

PatternVu [4] adds several powerful processing functions to the BERTScope:

- CleanEye is an eye diagram display mode, which averages waveform data to present an eye diagram with the non-data-dependent jitter removed. This allows the user to view and measure data-dependent jitter such as Inter-Symbol Inference, giving an intuitive idea of the compensatable jitter present, for example. It is effective on any repeating pattern up to 32,768 bits long.

- Single value waveform export is a utility which converts the CleanEye output to an export file in Comma Separated Vector (CSV) format. The output file, of up to 105 bit points, can then be imported into Microsoft Excel or software analysis and simulation tools such as Stateye or MATLAB®. This allows offline filtering of real captured data and the implementation of standards-based processing such as Transmitter Waveform Dispersion Penalty (TWDP) required by 802.3aq, the recent Long Reach MultiMode (LRM) 10 Gb Ethernet standard.

- The FIR filter equalization processor allows the emulation of the communication channel to view and measure the eye as the detector in the receiver would, by applying a software linear filter to the data before it is displayed. For example, the FIR Filter can be used to emulate the lossy effects of a backplane channel, or alternatively, emulate the receiver's equalization filter, facilitating the design and characterization of receiver-side equalization.

  The filter characteristics are controlled by entering the individual weighting coefficients of a series of taps in the FIR filter. Up to 32 taps with tap spacing from 0.1 to 1.0 unit intervals (UI) can be programmed to allow fine resolution of the filter shape. The FIR Filter can be applied to repeating patterns up to 32,768 bits long.

- Single edge jitter measurement allows truly deep BER-based jitter measurements to be applied to individual data edges at data rates above 3 Gb/s. The Single Edge Jitter Peak measurement function enables computation of jitter on a user-selectable single edge in the pattern, for repeating patterns up to 32,768 bits long. The resulting jitter measurement excludes data-dependent effects, showing only the uncorrelated jitter components such as Random Jitter (RJ), Bounded Uncorrelated Jitter (BUJ), and Periodic Jitter (PJ).

- Flexible measurements enables users to specify exactly the portion of the CleanEye waveform to use for accurate measurement of amplitude, rise and fall time, and de-emphasis ratio. Preprogrammed formulas for standards such as PCI Express and USB 3.1 are included.

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4   PatternVu operates at data rates of 900 Mb/s and higher.

Error analysis

Error analysis is a powerful series of views that associate error occurrences so that underlying patterns can be easily seen. It is easy to focus in on a particular part of an eye diagram, move the sampling point of the BERTScope there, and then probe the pattern sensitivity occurring at that precise location. For example, it is straightforward to examine which patterns are responsible for late or early edges.

Many views come standard with the BERTScope Family:

- Error statistics: A tabular display of bit and burst error counts and rates
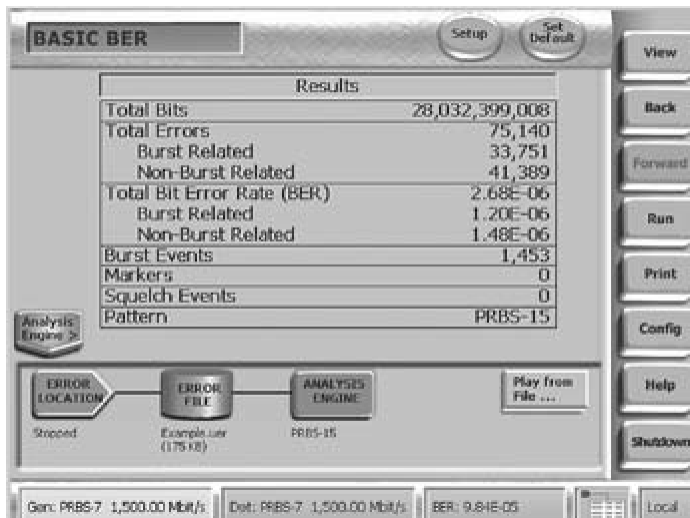
Error Statistics view showing link performance in terms of bit and burst occurrences.

- Strip chart: A strip chart graph of bit and burst error rates
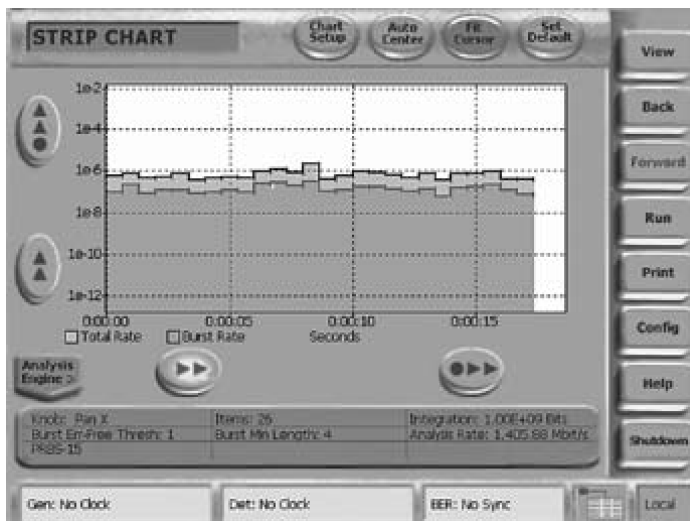
Strip Chart view showing bit and burst error performance over time. This can useful while temperature cycling as part of troubleshooting.

- Burst length: A histogram of the number of occurrences of errors of different lengths

- Error free interval: A histogram of the number of occurrences of different error-free intervals

- Correlation: A histogram showing how error locations correlate to user-set block sizes or external marker signal inputs

- Pattern sensitivity: A histogram of the number of errors at each position of the bit sequence used as the test pattern

- Block errors: A histogram showing the number of occurrences of data intervals (of a user-set block size) with varying numbers of errors in them
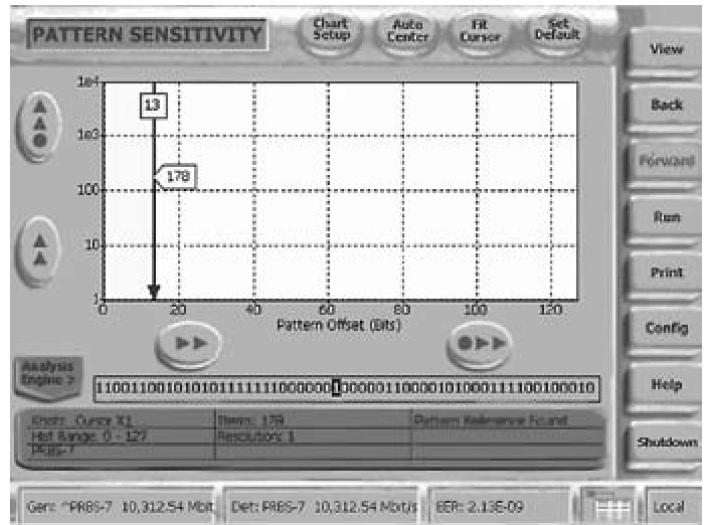
The Pattern Sensitivity view is a powerful way of examining whether error events are pattern related. It shows which pattern sequences are the most problematic, and operates on PRBS and user-defined patterns.

Error analysis options

Forward error correction emulation

Because of the patented error location ability of the BERTScope, it knows exactly where each error occurs during a test. By emulating the memory blocks typical of block error correcting codes such as Reed-Solomon architectures, bit error rate data from uncorrected data channels can be passed through hypothetical error correctors to find out what a proposed FEC approach would yield. Users can set up error correction strengths, interleave depths, and erasure capabilities to match popular hardware correction architectures.

2-D error mapping

This analysis creates a two-dimensional image of error locations from errors found during the test. Error mapping based on packet size or multiplexer width can show if errors are more prone to particular locations in the packet or particular bits in the parallel bus connected to the multiplexer. This visual tool allows for human eye correlation, which can often illuminate error correlations that are otherwise very difficult to find – even with all the other error analysis techniques.

Error location capture

Characteristic	Description
Live analysis	Continuous
Error logging capacity	Maximum 2 GB file size
Error events/second	10,000
Maximum burst length	32 kb

Jitter tolerance template option

Many standards call for SJ to be stepped through a template with different SJ amplitudes at particular modulation frequencies. This is easy with the built-in Jitter Tolerance function which automatically steps through a template that you designed, or one of the many standard templates in the library.

Standard library of templates:

- 10GBASE LX4 802.3ae 3.125 Gb/s
- 10 GbE 802.3ae 10.3125 Gb/s
- 40 GbE 802.3ba LR4 10.3125 Gb/s
- 100 GbE 802.3ba LR4/ER4 25.78125 Gb/s
- CEI 11G Datacom Rx Ingress (D) 11 Gb/s
- CGE Telecom Rx Egress (Re) 11 Gb/s [5]
- CEI 11G Telecom Rx Ingress (Ri) 11 Gb/s [5]
- CEI 11G Total Wander 11.1 Gb/s
- CEI 11G Total Wander 9.95 Gb/s
- CEI 6G Total Wander 4.976 Gb/s
- CEI 6G Total Wander 6.375 Gb/s
- CEI 25G Total Wander 25.78125 Gb/s
- FBB DIMM1 3.2 Gb/s
- FBB DIMM1 4.0 Gb/s
- FBB DIMM1 4.8 Gb/s
- FBB DIMM2 3.2 Gb/s
- FBB DIMM2 4.0 Gb/s
- FBB DIMM2 4.8 Gb/s

- Fibre Channel 1.0625 Gb/s
- Fibre Channel 2.125 Gb/s
- Fibre Channel 4.25 Gb/s
- Fibre Channel 8G 8.5 Gb/s
- Fibre Channel 16G 14.025 Gb/s
- OTN OTU-1 2.666G [5]
- OTN OTU-2 10.709 Gb/s
- OTN(10BASE-R) 11.1 Gb/s
- SAS (SCSI) 1.5 Gb/s
- SAS (SCSI) 3 Gb/s
- SDH 0.172 STM-1 155M [5]
- SDH 0.172 STM-16 2.4832 Gb/s [5]
- SDH 0.172 STM-4 622 Mb/s [5]
- SDH 0.172 STM-64 9.956 Gb/s [5]
- SDH STM-16 2.48832 Gb/s [5]
- SDH STM-64 9.9532 Gb/s [5]
- SONET OC-48 2.48832 Gb/s [5]
- SONET OC12 622 Mb/s [5]
- SONET OC192 9.9532 Gb/s [5]
- SONET OC192 9.95 Gb/s [5]
- SONET OC3 155 Mb/s [5]
- SONET OC48 2.4832 Gb/s [5]
- USB 3.1 5 & 10 Gb/s
- XAUI 3.125 Gb/s
- XFI ASIC Rx In Datacom (D) 10.3125 Gb/s
- XFI ASIC Rx In Datacom (D) 10.519 Gb/s
- XFI ASIC Rx In Telecom (D) 10.70 Gb/s
- XFI ASIC Rx In Telecom (D) 9.95328 Gb/s [5]
- XFI Host Rx In Datacom (C) 10.3125 Gb/s
- XFI Host Rx In Datacom (C) 10.519 Gb/s
- XFI Host Rx In Telecom (C) 10.70 Gb/s [5]
- XFI Host Rx In Telecom (C) 9.95328 Gb/s [5]
- XFI Module Tx In Datacom (B') 10.3125 Gb/s
- XFI Module Tx In Datacom (B') 10.519 Gb/s
- XFI Module Tx In Telecom (B') 10.70 Gb/s [5]
- XFI Module Tx In Telecom (B') 9.95328 Gb/s [5]

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[5]   Requires Option XSSC.

Some of the areas of adjustment include:

- BER confidence level
- Test duration per point
- BER threshold
- Test device relaxation time
- Imposition of percentage margin onto template
- Test precision Control over A/B Pattern switch behavior

Also included is the ability to test beyond the template to device failure at each chosen point, and the ability to export data either as screen images or CSV files.

Jitter map option

The Jitter map [6] option provides automated jitter decomposition with long pattern jitter triangulation. It extends BER-based jitter decomposition beyond Dual Dirac measurement of Total Jitter (TJ), Random Jitter (RJ), and Deterministic Jitter (DJ) to a comprehensive set of subcomponents. It can also measure and decompose jitter on extremely long patterns, such as PRBS-31, providing that it can first run on a shorter synchronized data pattern.

The option includes the following features:

- DJ breakdown into Bounded Uncorrelated Jitter (BUJ), Data Dependent Jitter (DDJ), Inter-Symbol Interference (ISI), Duty Cycle Distortion (DCD), and Sub-Rate Jitter (SRJ) [7] including F/2 (or F2) jitter
- BER based for direct (non-extrapolated) Total Jitter (TJ) measurement to 10^{-12} BER and beyond
- Separation of correlated and uncorrelated jitter components eliminates mistaking long pattern DDJ for RJ
- Visualization of RJ RMS measured on individual edges of the data pattern
- J2 and J9 jitter measurements for 100 GbE applications

- Additional levels of breakdown not available from other instruments such as: Emphasis Jitter (EJ), Uncorrelated Jitter (UJ), Data Dependent Pulse Width Shrinkage (DDPWS), and non-ISI
- Intuitive, easy-to-navigate jitter tree

Stressed live data option

The BERTScope Stressed Live Data software option enables engineers to add various types of stress to real data traffic in order to stress devices with bit sequences representative of the environment they will encounter once deployed. Using live traffic with added stress tests the boundaries of device performance and lends added confidence to designs before they are shipped.

- Full range of calibrated stress available on the BERTScope, including Sinusoidal Jitter (SJ), Random Jitter (RJ), Bounded Uncorrelated Jitter (BUJ), Sinusoidal Interference (SI), F/2 Jitter, and Spread Spectrum Clocking (SSC)
- Data rate support up to the maximum of the BERTScope
- Full-rate clock required up to 11.2 Gb/s, half-rate clock required above 11.2 Gb/s

Symbol filtering option

Symbol filtering enables asynchronous BER testing, including Jitter Tolerance testing, on incoming data streams that have a nondeterministic number of clock compensation symbols inserted into the bit stream, as is common in 8b/10b encoded systems when placed in loopback for receiver testing.

- Supports asynchronous receiver testing for USB 3.1, SATA, and PCI Express
- User-specified symbols are automatically filtered from the incoming data to maintain synchronization
- The Error Detector maintains a count of filtered bits for accurate BER measurement

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6   Jitter map operates at data rates of 900 Mb/s and higher.

7   SRJ and F/2 jitter operate up to 8.5 Gb/s (BSA85C), 11.2 Gb/s (BSA125C, BSA175C, BSA286CL).

Pattern generator specifications

All specifications apply to all models unless noted otherwise.

Data outputs

Data rate range	
BSA85C	0.1 to 8.5 Gb/s
BSA125C	0.1 to 12.5 Gb/s
BSA175C	0.5 to 17.5 Gb/s
BSA286CL	1 to 28.6 Gb/s
Format	NRZ
Polarity	Normal or inverted
Variable cross over	25 to 75%
Patterns	
Hardware patterns	Industry-standard Pseudo-random (PRBS) of the following types: $2^n - 1$ where n = 7, 11, 15, 20, 23, 31
RAM patterns	128 bits to 128 Mb total, allocated in 32 Mb portions to each of two A/B pages. Single page max is 128 Mb
Library	Wide variety including SONET/SDH, Fibre Channel based such as k28.5, CJTPAT; 2^n patterns where n = 3, 4, 5, 6, 7, 9; Mark Density patterns for 2^n where n = 7, 9, 23; and many more
Error insertion	
Length	1, 2, 4, 8, 16, 32, 64 bit bursts
Frequency	Single or repetitive

Clock outputs

Frequency range	Rise times are measured 20% to 80% unless otherwise stated. Specifications are following a 20-minute warm-up period. Specifications subject to change.
BSA85C	0.1 to 8.5 GHz
BSA125C	0.1 to 12.5 GHz [8]
BSA175C	0.5 to 17.5 GHz [8]
BSA286CL	1-28.6 GHz [8]
Phase noise	< –90 dBc/Hz at 10 kHz offset (typical)
Clock output divide ratios	Opt. STR only (See the *Clock path details* below.)

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[8]   Clock output frequency is ÷2 at data rates above 11.2 Gb/s.

Data clock amplitudes and offsets

Configuration	Differential outputs, each side of pair individually settable for termination, amplitude, offset
Interface	DC coupled, 50 Ω reverse terminated, 3.5 mm connector. Calibration into 75 Ω selectable, other impedances by keypad entry. User-replaceable Planar Crown® adapter allows change to other connector types
Preset logic families	LVPECL, LVDS, LVTTL, CML, ECL, SCFL
Terminations	Variable, –2 to +2 V Presets: +1.5, +1.3, +1, 0, –2 V, AC coupled
Allowable amplitudes, terminations, and offsets	Refer to the following figures.
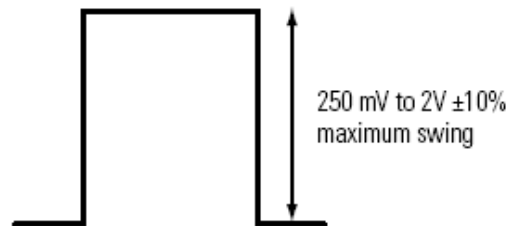
Amplitude swings between 0.25 and 2.0 V allowed; should fit inside shaded area of the following graph. For example, SCFL uses a 0 V termination, and operates between approximately 0 and –0.9 V; as shown with dotted arrow, it falls within the operating range.

Datasheet
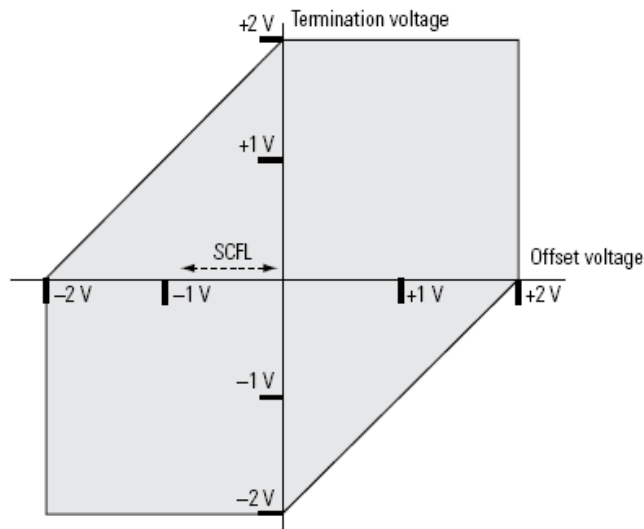
Data clock waveform performance

Rise time	25 ps max, 23 ps typical (10-90%), 1 V amplitude, at 8.0 Gb/s

Jitter	
BSA85C	≤12 ps_{p-p} TJ (@8.0 Gb/s) typical
	≤700 fs RMS Random Jitter (@8.0 Gb/s) typical
BSA125C, BSA175C	<500 fs RMS Random Jitter (@10.3125 Gb/s) typical
BSA286CL	≤8 ps_{p-p} TJ (@28.05 Gb/s) typical
	≤300 fs RMS Random Jitter (@28.05 Gb/s) typical

Clock/data delay

Range	Greater than 1 bit period in all cases
Up to 1.1 GHz	30 ns
Above 1.1 GHz	3 ns

Resolution	100 fs

Self calibration	At time of measurement, when temperature or bit rate are changed, instrument will recommend a self calibration. Operation takes less than 10 seconds.

Pattern generator front panel connections

External clock inputs

Allows use of an external clock source to clock the BERTScope. Models equipped with stress are able to add impairments to incoming clock, including when external signal has Spread Spectrum Clocking (SSC) in excess of 5000 ppm imposed on it.

Frequency range	
BSA85C	0.1 to 8.5 GHz
BSA125C	0.1 to 12.5 GHz
BSA175C	0.5 to 17.5 GHz
BSA286CL	1 to 28.6 GHz
Nominal power	900 mV$_{p-p}$ (+3 dBm)
Maximum power	2.0 V$_{p-p}$ (+10 dBm)
Return loss	Better than –6 dB
Interface	50 Ω SMA female, DC coupled into selectable termination voltage

HF Jitter (Opt. STR only)

One of two jitter insertion inputs. Can be used to insert SJ, RJ, BUJ if desired.

Frequency range	DC to 1.0 GHz
Jitter amplitude range	Up to 0.5 UI maximum
Input voltage range	0-2 V$_{p-p}$ (+10 dBm) for normal operation
	6.3 V$_{p-p}$ (+20 dBm) max nondestructive input
Data rate range	Limited performance to 622 Mb/s (BSA286CL excluded)
BSA85C	1.5 to 8.5 Gb/s
BSA125C	1.5 to 12.5 Gb/s
BSA175C	1.5 to 17.5 Gb/s
BSA286CL	1.5 to 28.6 Gb/s
Interface	SMA female, 50 Ω, DC coupled into 0 V

Sub-rate clock outputs

BERTScope standard models have clock divided by 4. BERTScope Option STR models have additional capabilities.

Frequency range	Model	Standard range	Range with Opt. STR
	BSA125C	0.025 to 2.125 GHz	8.5 GHz
		0.025 to 2.8 GHz	11.2 GHz
	BSA175C	0.125 to 2.8 GHz	11.2 GHz
	BSA286CL	0.250 to 3.575 GHz	14.3 GHz

Amplitude range	0.6 V_{p-p}, nominal, centered around 0 V
Transition time	<500 ps
Interface	SMA female, 50 Ω, DC coupled into 0 V

Trigger output

Provides a pulse trigger to external test equipment. It has two modes:

 Divided Clock Mode: Pulses at 1/256th of the clock rate

 Pattern Mode: Pulse at a programmable position in the pattern (PRBS), or fixed location (RAM patterns)

Stress modulation added on models so equipped, when enabled.

Minimum pulse width	128 Clock Periods (Mode 1)
	512 Clock Periods (Mode 2)
Transition time	<500 ps
Jitter (p-p, data to trigger)	<10 ps, typical (BSA175C, BSA286CL)
Output levels	CML; >300 mV_{p-p}, center around -250 mV
Interface	50 Ω SMA female

Pattern generator rear panel connections

Pattern start input

For users wanting to synchronize patterns of multiple data streams from multiple instruments simultaneously.

Logic levels	LVTTL (<0.5 V Low, >2.5 V High)
Threshold	+1.2 V typical
Maximum nondestructive input range	–0.5 V to +5.0 V
Minimum pulse width	128 serial clock periods
Maximum repetition rate	512 serial clock periods
Interface	SMA female, >1 kΩ impedance into 0 V

Page select input

In A-B Page Select mode, allows external control of the pattern. Software control over rising or falling edge trigger, continuous Pattern B after completion of Pattern A, or run B only once before reverting back to A.

Logic levels	LVTTL (<0.5 V Low, >2.5 V High)
Threshold	+1.2 V typical
Maximum nondestructive input range	–0.5 V to +5.0 V
Minimum pulse width	1 pattern length
Interface	SMA female, >1 kΩ impedance into 0 V

Sinusodial interference output (Opt. STR only)

SI output from internal generator. Can be used to apply SI after external ISI channel.

Frequency range	0.1-2.5 GHz
Output voltage	0-3 $V_{p\text{-}p}$
Interface	SMA Female, 50 Ω, AC coupled

Low frequency jitter input (Opt. STR only)

	Allows use of external low-frequency jitter source to modulate the stressed Pattern Generator output.
Frequency range	DC to 100 MHz
Jitter amplitude range	Up to 1.1 ns, can be combined with other internal low-frequency modulation
Input voltage range	0-2 V_{p-p} (+10 dBm) for normal operation
	6.3 V_{p-p} (+20 dBm) maximum nondestructive input
Data rate range	
BSA85C	Up to 8.5 Gb/s
BSA125C	Up to 12.5 Gb/s
BSA175C	Up to 17.5 Gb/s
BSA286CL	Up to 28.6 Gb/s
Interface	SMA female 50 Ω, DC coupled into 0 V

Low frequency sinusoidal jitter output (Opt. STR only)

	To allow phasing of two BERTScopes together, in-phase or anti-phase.
Frequency range	As set for internal SJ from user interface
Amplitude	2 V_{p-p}, centered at 0 V
Interface	SMA female, 50 Ω, AC coupled

Reference input

	To lock the BERTScope to an external frequency reference from of another piece of equipment.
Frequency	10 MHz, 100 MHz, 106.25 MHz, 133.33 MHz, 156.25 MHz, 166.67 MHz, or 200 MHz
Amplitude	0.325 to 1.25 V_{p-p} (–6 to +6 dBm)
Interface	50 Ω SMA female, AC coupled

Reference output

|	Provides a frequency reference for other instruments to lock to.
Configuration	(BSA125C) Differential
	Single Ended (Ref-Out not used) for all models other than BSA125C
Frequency	10 MHz, 100 MHz, 106.25 MHz, 133.33 MHz, 156.25 MHz, 166.67 MHz, or 200 MHz
Amplitude	1 V_{p-p} (+4 dBm) nominal, each output, (2 V_{p-p} differential)
Interface	50 Ω SMA female, AC coupled

Clock path details

BSA85C
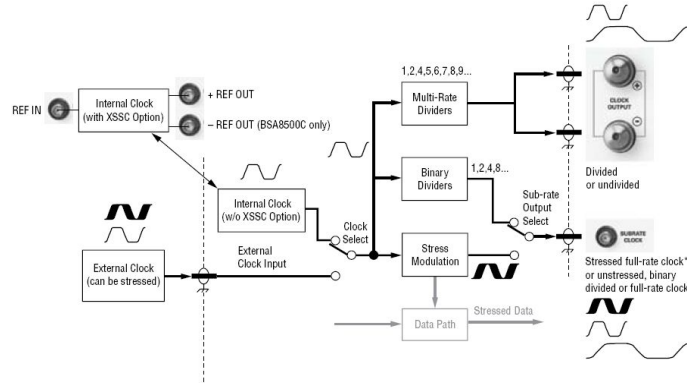
Functional block diagram of the clock path for models with stress capability, BSA85C.

** Stress may be added to an external clock on appropriate models. Stress operating range is from 1.5 to 11.2 Gb/s. External clock must have a duty cycle of 50% ±2%.
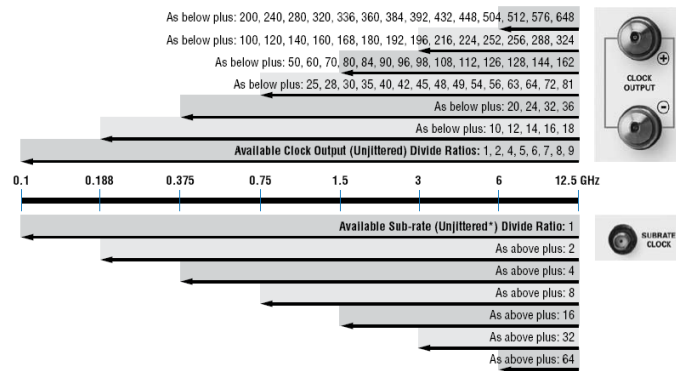
Available divide ratios from clock-related output, by bit rate, using the internal clock, BSA85C. All listed ratios available for an external clock input over entire bit rate range, limitations for internal clock only. Minimum specified frequency of the clock output is 100 MHz. Operation below this rate will be uncalibrated.

* The Sub-rate clock output can also provide a full-rate jittered clock.

Clock path details

BSA125C, BSA175C, BSA286CL

Functional block diagram of the clock path for models with stress capability: BSA125C, BSA175C, BSA286CL.

** Stress may be added to an external clock on appropriate models. Stress operating range is from 1.5 to 11.2 Gb/s. External clock must have a duty cycle of 50% ±2%.
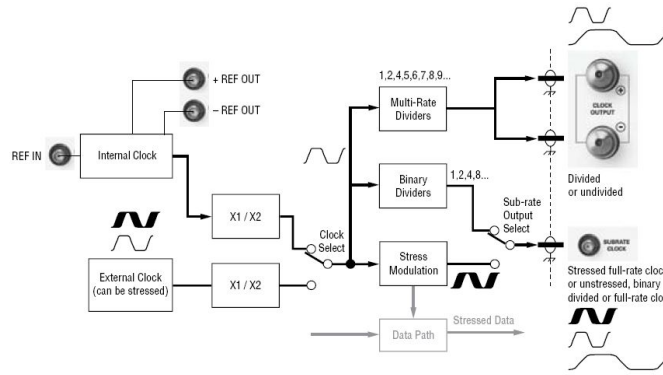
The BSA125C, BSA175C, and BSA286CL models use an internal Double Data Rate (DDR) architecture to operate at data rates ≥11.2 Gb/s. When operating at 11.2 Gb/s or higher data rate, the clock output will be 1/2 the data rate. The external clock can be specified to be either full or half data rate. When full rate is selected, the pattern generator will operate in DDR mode when the input clock frequency is 11.2 GHz or higher.

These ratios apply to operation from internal clock only. The external clock will be output at 1/2 rate when half rate is selected, or when full rate is selected and clock rate is ≥11.2 GHz.

The minimum data rate specified for the main clock output is 500 Mb/s. Output will be uncalibrated when operated at divided rates lower than 500 Mb/s.

Clock path details

Multi-rate and sub-rate divider ratios for main clock output

Only applies to BSA125C, BSA175C, and BSA286CL

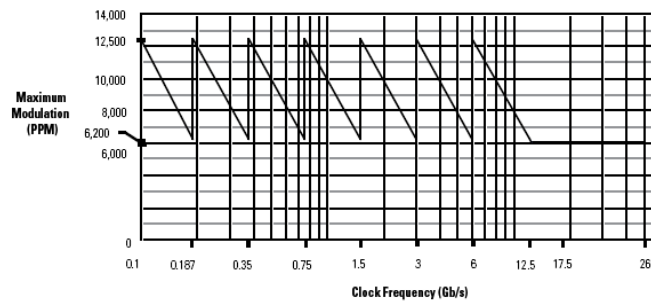| Data rate (Gb/s)	Ratios for main clock output	Ratios for sub-rate clock output [10]
500-750 Mb/s	1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 32, 36	1, 2, 4
0.75-3 Gb/s	1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 30, 32, 32, 35, 36, 36, 40, 42, 45, 48, 50, 54, 56, 60, 64, 70, 72, 80, 81, 84, 90, 98, 108, 112, 126, 128, 144, 162	1, 2, 4, 8
3-6 Gb/s	1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 30, 32, 32, 35, 36, 36, 40, 42, 45, 48, 50, 54, 56, 60, 64, 70, 72, 80, 81, 84, 90, 98, 100, 108, 112, 120, 126, 128, 140, 144, 160, 162, 168, 180, 192, 196, 216, 224, 252, 256, 288, 324	1, 2, 4, 8, 16, 32
6-11.2 Gb/s	1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 30, 32, 32, 35, 36, 36, 40, 42, 45, 48, 50, 54, 56, 60, 64, 70, 72, 80, 81, 84, 90, 98, 108, 112, 126, 128, 140, 144, 144, 160, 162, 162, 168, 180, 192, 196, 200, 216, 224, 240, 252, 256, 280, 288, 320, 324, 360, 384, 392, 432, 448, 504, 512, 576, 648	1, 2, 4, 8, 16, 32, 64
11.2-12 Gb/s	2, 4, 8, 10, 12, 14, 16, 18, 20, 24, 28, 32, 36, 40, 48, 60, 64, 64, 70, 72, 72, 80, 84, 90, 96, 100, 108, 112, 120, 128, 140, 144, 160, 162, 168, 180, 196, 200, 216, 224, 240, 252, 256, 280, 288, 320, 324, 336, 360, 384, 392, 432, 448, 504, 512, 576, 648	2, 4, 8, 16, 32, 64
12-26 Gb/s	2, 4, 8, 10, 12, 14, 16, 18, 20, 24, 28, 32, 36, 40, 48, 60, 64, 64, 70, 72, 72, 80, 84, 90, 96, 100, 108, 112, 120, 128, 140, 144, 160, 162, 168, 180, 196, 216, 224, 252, 256, 280, 288, 288, 320, 324, 324, 336, 360, 384, 392, 400, 432, 448, 480, 504, 512, 560, 576, 640, 648, 720, 768, 784, 864, 896, 1008, 1024, 1152, 1296	2, 4, 8, 16, 32, 64, 128

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[10] Sub-rate clock connector can also output a full-rate stressed clock up to 11.2 Gb/s, or half-rate stressed clock at rates ≥11.2 Gb/s.

Additional stress options

Enhanced spread spectrum clock option (Opt. STR and/or Opt. XSSC)

Adds a modulator directly to the synthesizer clock output – modulation affects main and sub-rate clock output (regardless of the state of sub-rate output select), Data Output, and Trigger Output.

|	
Modes	SSC or Phase Modulation (sinusoidal)
Data rate range	Full range of BERTScope
SSC wave shape	Triangle or Sine
SSC frequency range	20 kHz to 40 kHz
SSC modulation range	12,500 ppm at 6 Gb/s 6,200 ppm at 12 Gb/s 6,000 ppm at 12.5 Gb/s and above See Maximum SSC Modulation graph for range at lower clock rates Maximum SSC modulation with Option XSSC
SSC modulation resolution	1 ppm
SSC modulation type	Down Spread, Center Spread, Up Spread
PM frequency range	10 Hz to 160 kHz
PM frequency resolution	1 Hz

Data rate	Maximum modulation
>6 Gb/s	6000 UI
3 to 6 Gb/s	3000 UI
1.5 to 3 Gb/s	1500 UI
0.75 to 1.5 Gb/s	750 UI
375 to 750 Mb/s	375 UI
187 to 375 Mb/s	187.5 UI
100 to 187 Mb/s	93.75 UI
Reduced for modulation frequencies >2 kHz	See Phase Modulation Range graph.

PM modulation range -- for modulation frequency 10 Hz to 2 kHz
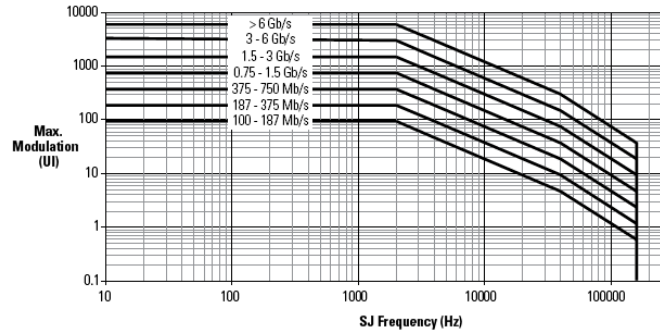
Phase Modulation Range with Option XSSC

F/2 jitter generation option (Opt. F2, also requires Opt. STR)

F/2 or sub-rate jitter is found in high data rate systems which multiplex up 2 or more lower data rate streams. The jitter results for lack of symmetry in the multiplexing clock, giving all of the even bits different pulse width than the odd bits. Unlike conventional DCD, F/2 jitter is independent of the logic state of the bit. F/2 jitter is part of the stress recipe used in testing compliance to some of the newer standards such as 802.3ap (10 Gb backplane Ethernet).

Supported data rates   8.0 and 10.3125 Gb/s

Modulation range   0-5.0% UI

Extended stress generation option (Opt. PCISTR)

This option adds additional stress generators required for compliance testing receivers to PCIe 2.0 specifications, internal to the BERTScope.

Clock frequency range   Up to 11.2 Gb/s

LFRJ modulation range   0-1.1 ns [11]

LFRJ frequency range   Band-limited to 10 kHz - 1.5 MHz, with roll off to PCIe 2.0 specifications

LFSJ modulation range   0-368 ps [11] at 5 Gb/s

LFSJ frequency range   1-100 kHz

The Extended Stress option also adds selectable bandwidth-limiting to the normal, broadband RJ generator.

[11]   Can be combined with other low-frequency modulation.

Extended stress generation option (Opt. PCISTR)

RJ frequency, Normal mode	Band-limited to 10 MHz - 1 GHz
RJ frequency, PCIE mode	Band-limited to 1.5-100 MHz with roll off to PCIe 2.0 specifications

Error detector specifications

Clock input

Configuration	Single ended
Frequency range	
BSA85C	0.1 to 8.5 Gb/s
BSA125C	0.1 to 12.5 Gb/s
BSA175C	0.5 to 17.5 Gb/s [12]
BSA286CL	1 to 28.6 Gb/s [13]

Data and clock interfaces

Connector	3.5 mm
Impedance	50 Ω
Threshold voltage	–2 to +3.5 V
Threshold presets	LVPECL, LVDS, LVTTL, CML, ECL, SCFL
Terminations	Variable, –2 V to +3 V
	Presets: +1.5, +1.3, +1, 0, –2 V, AC coupled
Maximum nondestructible input	$-3\ V_{peak}$, $+4\ V_{peak}$, applied to any connector

Detector clock data delay

Range	Greater than 1 bit period in all cases
Up to 1.1 GHz	30 ns
Above 1.1 GHz	3 ns
Resolution	100 fs
Self calibration	Supported – At time of measurement, when temperature or bit rate are changed, instrument will recommend a self calibration. Operation takes less than 10 seconds.

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[12]   A full- or half-rate clock may be used for data rates above 11.2 Gb/s.

[13]   From 26 to 28.6 Gb/s the input detector operates at half rate (using even or odd bits).

Data inputs

Data rate range	
BSA85C	0.1 to 8.5 Gb/s
BSA125C	0.1 to 12.5 Gb/s
BSA175C	0.5 to 17.5 Gb/s
BSA286CL	1 to 28.6 Gb/s
Configuration	Differential
Format	NRZ
Polarity	Normal or Inverted
Threshold alignment	Can auto-align to differential crossing point
Sensitivity	
Single ended	100 mV$_{p\text{-}p}$, typical
Differential	50 mV$_{p\text{-}p}$, typical
Maximum input signal swing	2 V$_{p\text{-}p}$
Intrinsic transition time	16 ps typical, 10/90%, single ended (equivalent to >20 GHz detector bandwidth). Measured at input, ECL levels
Hardware patterns	Industry-standard Pseudo-random (PRBS) of the following types: $2^n - 1$ where n = 7, 11, 15, 20, 23, 31
RAM patterns	
User defined	128 bits to 128 Mb, 128-bit increments
Library	Wide variety including SONET/SDH, Fibre Channel based such as k28.5, CJTPAT; 2^n patterns where n = 3, 4, 5, 6, 7, 9; Mark Density patterns for 2^n where n = 7, 9, 23; and many more
RAM pattern capture	Capture incoming data up to 128 Mb in length. Edit captured data, send to Pattern Generator, Error Detector, or both
RAM pattern capture modes	
Capture by length	1 to 1,048,576 words. 1-word default. Words 128 bit in length
Capture by triggers	Captures when "Detector Start" on rear panel goes high, to maximum allowable length or until input goes low
Capture by length from trigger	Capture by length initiated from "Detector Start" input, to pre-specified length

Datasheet

Data inputs

Synchronization -- Auto-resync   User-specified number of 128 bit words containing 1 or more errors per word initiates a re-sync attempt
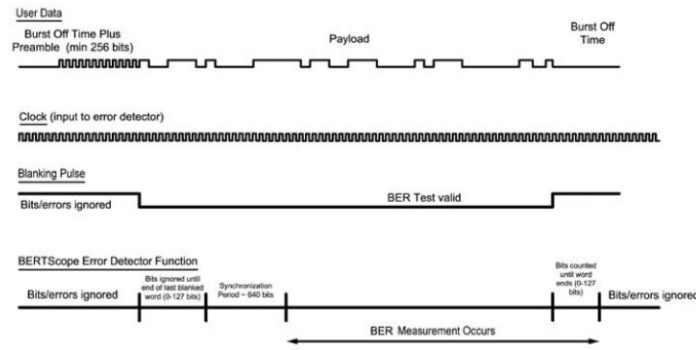
BERTScope Burst Analysis Timing – BERTScope word size is 128 bits. An example timing diagram is shown here for a PRBS payload. Counting of bits will not start until a 128-bit word boundary occurs, meaning that after the blanking pulse transitions, up to 127 bits may pass before synchronization begins. For a PRBS, synchronization typically takes 5 words, or 640 bits. Similarly, bit measurement will continue for up to 127 bits after the blanking signal transitions again. RAM-based patterns take longer to synchronize.

Manual synchronization   User initiates re-sync.

Pattern matching synchronization

    Grab 'n' go   Error Detector captures specified pattern length and compares next instances to find match (Fast method, but susceptible to ignoring logical errors).

    Shift-to-sync   Error Detector compares incoming pattern with reference RAM pattern, looks for match, if none found shifts pattern by one bit and compares again (slower, but most accurate method).

Error detector basic measurements   BER, Bits Received, Re-syncs, Measured Pattern Generator and Error Detector Clock Frequencies

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Error detector front panel connections

Error correlation marker input

Allows an external signal to provide a time-tagged marker to be placed in the error data set.

Logic family	LVTTL (<0.5 V Low, >2.5 V High)
Threshold	+1.2 V
Minimum pulse width	128 clock periods
Maximum repetition rate	512 serial clock periods
Maximum frequency	<4000 markers/s recommended
Interface	BNC female, >1 kΩ impedance into 0 V

Blank input

Useful for recirculating loop fiber experiments or during channel training sequences. Causes errors to be ignored when active. Bit count, error count, and BER not counted. No re-sync occurs when counting is re-enabled.

Logic family	LVTTL (<0.5 V Low, >2.5 V High)
Threshold	+1.2 V
Minimum pulse width	128 clock periods
Maximum repetition rate	512 serial clock periods
Interface	BNC female, >1 kΩ impedance into 0 V

Error output

Provides a pulse when an error is detected. Useful for triggering an alarm while doing long-term monitoring.

Minimum pulse width	128 clock periods
Transition time	<500 ps
Output levels	1000 mV nominal (0 V to 1 V low-high)
Interface	SMA female

Trigger output

Provides a pulse trigger to external test equipment. It has two modes:

Divided Clock Mode: Pulses at 1/256th of the clock rate.

Pattern Mode: Pulse at a programmable position in the pattern (PRBS), or fixed location (RAM patterns).

Minimum pulse width	128 clock periods (Mode 1)
	512 clock periods (Mode 2)
Transition time	<500 ps
Output levels	>300 mV amplitude, 650 mV offset
Interface	50 Ω SMA female

Error detector rear panel connections

Detector start input

Used to trigger the acquisition of incoming data into the Error Detector reference pattern memory. High level starts capture.

Amplitude	LVTTL (<0.5 V Low, >2.5 V High)
Threshold	+1.2 V
Minimum pulse width	128 serial clock periods
Minimum repetition rate	512 serial clock periods
Interface	SMA female, >1 kΩ impedance into 0 V

General specifications

All specifications apply to all models unless noted otherwise.

PC-related specifications

Display	TFT touch screen 640×480 VGA
Touch sensor	Analog resistive
Processor	Pentium® P4 1.5 GHz or greater
Hard disk drive	40 GB or greater
DRAM	1 GB
Operating system	Microsoft Windows 7 Professional

PC-related specifications

Remote control interfaces	IEEE-488 (GPIB) or TCP/IP
Supported interfaces	VGA display
	USB 2.0 (6 total, 2 front, 4 rear)
	100BASE-T Ethernet LAN
	IEEE-488 (GPIB)
	Serial RS-232

Physical characteristics

Height	220 mm (8.75 in.)
Width	394 mm (15.5 in.)
Depth	520 mm (20.375 in.)
Weight	
Instrument only	25 kg (55 lb.)
Shipping	34.5 kg (76 lb.)
Power	460 W
Voltage	100 to 240 VAC (±10%), 50 to 60 Hz

Environmental characteristics

Warm-up time	20 minutes
Operating temperature range	10 °C to 35 °C (50 °F to 95 °F)
Operating humidity	Noncondensing at 35 °C (95 °F), 15 to 65%
Certifications	EU EMC Directive (CE-Marked), LVD Low Voltage Directive, US Listed UL61010-1, Canada Certified CAN/CSA 61010-1

Ordering information

BERTScope BSA series models

All Models Include: user manual, power cord, mouse, three (3) short low-loss cables

BSA85C	Single channel, BERTScope 8.5 Gb/s Bit Error Rate Analyzer
BSA125C	BERTScope 12.5 Gb/s Bit Error Rate Analyzer
BSA175C	BERTScope 17.5 Gb/s Bit Error Rate Analyzer
BSA286CL	BERTScope 28.6 Gb/s Bit Error Rate Analyzer
BSA286CL-260 Opt: CA	BERTScope OPTIONS; Conversion of a BSA260C to a BSA286CL (Serial number range from 280500 to 280633, minus 280619 & 280629)
BSA286CL-260 Opt: CB	BERTScope OPTIONS; Conversion of a BSA260C to a BSA286CL (Serial number range from 280634 to 280699, plus 280619 & 280629)
BSA286CL-260 Opt: CC	BERTScope OPTIONS; Conversion of a BSA260C to a BSA286CL (Serial number range from 280700 and higher)

Clock recovery instruments

CR125A	12.5 Gb/s Clock Recovery Instrument
CR175A	17.5 Gb/s Clock Recovery Instrument
CR286A	28.6 Gb/s Clock Recovery Instrument

Digital pre-emphasis processors

DPP125C	1-12.5 Gb/s 3-Tap and optional 4-Tap Digital Pre-emphasis Processor

Instrument options

BSA options

Opt. F2	F/2 Jitter Generation at 8G/10.3125G (requires STR)
Opt. STR	Stressed Signal Generation (includes option ECC, MAP, PL, XSSC, JTOL)
Opt. XSSC	Extended Spread Spectrum Clocking (SSC) (included in STR)
Opt. PCISTR	Add PCIe Gen2 Extended Stress Generation
Opt. J-MAP	Add Jitter Decomposition SW
Opt. ECC	Add Error Correction Coding Emulation SW (included in STR)
Opt. JTOL	Add Jitter Tolerance Templates SW (included in STR)
Opt. LDA	Add Live Data Analysis SW
Opt. MAP	Add Error Mapping Analysis SW (included in STR)
Opt. PL	Add Physical Layer Test Suite SW (included in STR)
Opt. PVU	Add PatternVu Equalization Processing SW
Opt. SF	Add Symbol Filtering option SW (used with STR) [14]
Opt. SLD	Add Stressed Live Data option SW

Opt. CA1	Provides a single calibration event or coverage
Opt. C3	Calibration Service 3 Years
Opt. R3	Repair Service 3 Years (including warranty)
Opt. R3DW	Repair Service Coverage 3 Years (includes product warranty period). 3-year period starts at time of customer instrument purchase

Clock recovery instrument options

Option	Description	CR125A	CR175A	CR286A
PCIE	PCIe PLL analysis (requires jitter spectrum option, operates at 2.5G and 5G only)	X	X	X
PCIE8	PCIe PLL analysis (requires jitter spectrum option, operates at 2.5G, 5G, and 8G only)	X	X	X
HS	Add High Sensitivity Clock Recovery		X	X
XLBW	Add Extended Loop Bandwidth in the Clock Recovery	X	X	X
12GJ	Add 11.2G spectrum analysis to CR125A	X		
17GJ	Add 11.2G spectrum analysis to CR175A		X	
28GJ	Add 11.2G spectrum analysis to CR286A			X
CA1	Provides a single calibration event or coverage	X	X	X
C3	Calibration Service 3 Years	X	X	X
R3	Repair Service 3 Years (including warranty)	X	X	X
R3DW	Repair Service Coverage 3 Years (includes product warranty period). 3-year period starts at time of customer instrument purchase	X	X	X

Digital pre-emphasis processor options

Opt. 4T	4-Tap Digital Pre-emphasis Processor
Opt. ECM	Eye Opener, Clock Multiplier, Clock Doubler
Opt. CA1	Single Calibration or Functional Verification
Opt. C3	Calibration Service 3 Years
Opt. R3	Repair Service 3 Years (including warranty)
Opt. R5	Repair Service 5 Years (including warranty)
Opt. R3DW	Repair Service Coverage 3 Years (includes product warranty period). 3-year period starts at time of customer instrument purchase.

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14 This option is included with Option STR for the BSA85C instruments.

Recommended accessories

LE160/LE320	16 Gbps / 32 Gbps, 2-channel linear equalizers
CR125ACBL	High-performance Delay Matched Cable Set (required for BERTScope and CRU in SSC applications)
100PSRTFILTER	100 ps Rise Time Filter
BSA12500ISI	Differential ISI Board
PMCABLE1M	Precision Phase Matched Cable Pair, 1 m
SMAPOWERDIV	SMA Power Dividers
BSARACK	BSA-Rackmount Kits
BSAUSB31	Bundle of Instrument Switch with Cables and Automation Software (supports USB 3.1 5 & 10 Gb/s)
BSAUSB3	Bundle of Instrument Switch with Cables and Automation Software (supports USB 3.1 5 Gb/s)
BSASWITCH	Instrument Switch with Cables
BSAUSB3SFT	USB3 Automation Software

CE

Tektronix is registered to ISO 9001 and ISO 14001 by SRI Quality System Registrar.

Product(s) complies with IEEE Standard 488.1-1987, RS-232-C, and with Tektronix Standard Codes and Formats.

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