Tektronix Logic Analyzers

▶ TLA7Axx Logic Analyzer Modules

▶ The TLA Series logic analyzer modules offer the highest performance for today's demanding applications.

Today's digital design engineers face daily pressures to speed new products to the marketplace. The TLA7Axx Series logic analyzer modules answer the need with breakthrough solutions for the entire design team, providing the ability to quickly monitor, capture and analyze real-time digital system operation in order to debug, verify, optimize and validate digital systems.

Hardware developers, hardware/software integrators and embedded software developers will appreciate the range of capabilities of the TLA7Axx Series logic analyzer modules. Its broad feature set includes capturing and correlating elusive hardware and software faults; providing simultaneous state, high-speed timing, and analog analysis through the same probe; using deep state acquisition to find the cause of complex problems; real-time, non-intrusive software execution tracing that correlates to source code and to hardware events; and non-intrusive connectorless probing.

The TLA7Axx Series logic analyzer modules offer Tektronix' breakthrough MagniVu™ technology for providing high-speed sampling (up to 8 GHz) that dramatically changes the way logic analyzers work and enables them to provide startling new measurement capabilities.

The TLA7Axx modules offer high-speed state synchronous capture, high-speed timing capture and analog capture through the same set of probes. They capitalize on MagniVu technology to offer up to 125 ps timing on all channels, glitch and setup/hold triggering and display and timestamp that is always on at up to 125 ps resolution. The TLA7Axx also offers new capabilities to capture source synchronous applications.

▶ Features & Benefits

34/68/102/136 Channel Logic Analyzers with up to 256 Mb Depth

500 ps (2 GHz)/32 Mb Deep Memory Timing Analysis

MagniVu™ Acquisition Technology Provides up to 125 ps (8 GHz) Timing Resolution to Find Difficult Problems Quickly

Up to 800 MHz State Acquisition Analysis of Synchronous Digital Circuits

Simultaneous State, High-speed Timing, and Analog Analysis Through the Same Probe Pinpoints Elusive Faults Without Double Probing

Glitch and Setup/Hold Triggering and Display Finds and Displays Elusive Hardware Problems

Transitional Storage Extends the Signal Analysis Capture Time

Simultaneous Analog and Digital Measurements Through the Same Probe

Compression Probing System With 0.5 pF Capacitive Loading Eliminates Need For On-board Connectors, Minimizes Intrusion on Circuits and is Ideal for Differential Signal Applications

Broad Processor and Bus Support

▶ Applications

Hardware Debug and Verification

Processor/Bus Debug and Verification Including Source Synchronous Clocking

Embedded Software Integration, Debug and Verification

Tektronix

Enabling Innovation

▸ Characteristics

General

Number of Channels (all channels are acquired including clocks) –
TLA7AA1: 34 channels (2 are clock channels).
TLA7AA2, TLA7AB2: 68 channels (4 are clock channels).
TLA7AA3: 102 channels (4 are clock and 2 are qualifier channels).
TLA7AA4, TLA7AB4: 136 channels (4 are clock and 4 are qualifier channels).
Channel Grouping: No limit to number of groups or number of channels per group (all channels can be reused in multiple groups).

Module "Merging" –
Up to five 102 channel or 136 channel modules can be "merged" to make up to a 680 channel module. Merged modules exhibit the same depth as the lesser of the five individual modules. Word/setup-and-hold/glitch/transition recognizers span all five modules. Range recognizers limited to three module merge. Only one set of clock connections is required.

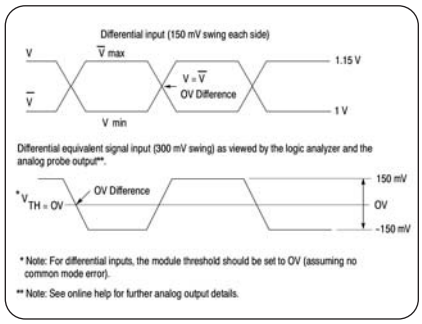
Time Stamp –
51-Bits at 125 ps resolution (3.25 days duration).

Clocking/Acquisition Modes –
Internal, internal 2X, internal 4X, external, external 2X, external 4X, source synchronous. 8 GHz MagniVu™ high-speed timing is available simultaneous with all modes.

Number of Mainframe Slots Required per TLA Series Module – 2.

▸ State Acquisition

Full Channel	Half Channel	Quarter Channel
120 MHz Standard	235 MHz/235 Mb/s or 240 Mb/s (DDR)	235 MHz/470 Mb/s
235 MHz Optional	450 MHz/450 Mb/s or 470 Mb/s (DDR)	450 MHz/900 Mb/s
450 MHz Optional	800 MHz/800 Mb/s or 900 Mb/s (DDR)	625 MHz/1.25 Gb/s



Input Characteristics (with P68xx or P69xx probes)

Capacitive Loading –
0.5 pF clock/data (P69xx).
<0.7 pF clock/data (P68xx).
(1.0 pF for P6810 in group configuration).

Threshold Selection Range –
From –2.0 V to +4.5 V in 5 mV increments. Threshold presets include TTL (1.5 V), CMOS (1.65 V), ECL (–1.3 V), PECL (3.7 V), LVPECL (2.0 V), LVCMOS 1.5 V (0.75 V), LVCMOS 1.8 V (0.9 V), LVCMOS 2.5 V (1.25 V), LVCMOS 3.3 V (1.65 V), LVDS (0 V) and user-defined.

Threshold Selection Channel Granularity –
Separate selection for each of the clock/qualifier channels and one per group of 16 data channels for each 34 channel probe.

Threshold Accuracy (including probe) –
±(35 mV + 1%).

Input Voltage Range –
Operating: –2.5 V to 5.0 V.
Nondestructive: ±15 V.

Minimum Input Signal Swing –
300 mV (single-ended).
$V_{MAX} - V_{MIN}$ >150 mV (differential).

Input Signal Minimum Slew Rate –
200 mV/ns typical.

State Acquisition Characteristics (with P68xx or P69xx probes)

State Memory Depth with Timestamps –
(quarter/half/full channels) 512/256/128 Kb, 2 Mb/1 Mb/512 Kb, 8/4/2 Mb, 32/16/8 Mb, 128/64/32 Mb, 256/128/64 Mb per channel.

Setup and Hold Time Selection Range –
From 16 ns before, to 8 ns after clock edge in 125 ps increments. Range may be shifted towards the setup region by 0 ns [+8, –8] ns, 4 ns [+12, –4] ns or 8 ns [+16, 0] ns.

Setup-and-hold Window –
All Channels: 625 ps typical.
Single Channel: 500 ps typical.

Minimum Clock Pulse Width –
500 ps (P6960, P6964, P6980, P6982, P6860, P6864, P6880), 700 ps (P6810).

Active Clock Edge Separation – 400 ps.

Demux Channel Selection –
Channels can be demultiplexed to other channels through user interface with 8 channel granularity.

Source Synchronous Clocking –
Up to four "Fast Latches" per module (20 max per 5-way merge) to strobe source-synchronous buses into TLA7Axx Modules.
Four sets of any predefined "Fast Latches" may be combined with qualification data and data pipelining to store four independent source-synchronous data buses.
Two "Fast Latches" may be combined to address DDR applications.

Timing Acquisition Characteristics (with P68xx or P69xx probes)

MagniVu™ Timing –
125 ps max, adjustments to 250 ps, 500 ps, 1 ns and 2 ns.
MagniVu Timing Memory Depth –
16 Kb per channel, with adjustable trigger position.
Deep Timing Resolution (quarter/half/full channels) –
500 ps/1 ns/2 ns to 50 ms.
Deep Timing Resolution with Glitch Storage Enabled – 4 ns to 50 ms.
Deep Timing Memory Depth (quarter/half/full channels with timestamps and with or without transitional storage) –
512/256/128 Kb, 2 Mb/1 Mb/512 Kb, 8/4/2 Mb, 32/16/8 Mb,128/64/32 Mb, 256/128/64 Mb per channel.
Deep Timing Memory Depth with Glitch Storage Enabled –
Half of default main memory depth.
Channel-to-channel Skew – 300 ps typical.
Minimum Recognizable Pulse/Glitch Width (single channel) –
500 ps (P6960, P6964, P6980, P6982, P6860, P6864, P6880), 750 ps (P6810).
Minimum Detectable Setup/Hold Violation – 250 ps.
Minimum Recognizable Multi-channel Trigger Event –
Sample period + channel-to-channel skew.

Analog Acquisition Characteristics (with P68xx or P69xx probes)

Bandwidth – 2 GHz typical.
Attenuation – 10x, ±1%.
Offset and Gain (Accuracy) –
±50 mV, +/–2% of Signal Amplitude.
Channels Demultiplexed – 4.
Run/Stop Requirements –
None, analog outputs are always active.
iView™ Analog Outputs –
Compatible with any internal TLA7Dx/Ex DSO module or supported TDS external oscilloscope.
iView Analog Output BNC Cable –
Low loss, 10x, 36-in.

Trigger Characteristics

Independent Trigger States – 16.
Maximum Independent If/then Clauses per State – 16.
Maximum Number of Events per If/then Clause – 8.
Maximum Number of Actions per If/then Clause – 8.
Maximum Number of Trigger Events –
18 (2 counter/timers plus any 16 other resources).
Number of Word Recognizers – 16.
Number of Transition Recognizers – 16.
Number of Range Recognizers – 4.
Number of Counter/Timers – 2.
Trigger Event Types –
Word, group, channel, transition, range, anything, counter value, timer value, signal, glitch, setup-and-hold violation, snapshot.
Trigger Action Types –
Trigger module, trigger all modules, trigger main, trigger MagniVu, store, don't store, start store, stop store, increment counter, decrement counter, reset counter, start timer, stop timer, reset timer, snapshot current sample, goto state, set/clear signal, do nothing.
Maximum Triggerable Data Rate –
1250 Mb/s (4X clocking mode).
Trigger Sequence Rate – DC to 500 MHz (2 ns).
Counter/Timer Range –
51 Bits each (>50 days at 2 ns).
Counter Rate – DC to 500 MHz (2 ns).
Timer Clock Rate – 500 MHz (2 ns).
Counter/Timer Latency – 2 ns.
Range Recognizers –
Double bounded (can be as wide as any group (408 channel max), must be grouped according to specified order of significance).
Setup-and-hold Violation Recognizer Setup Time Range –
From 8 ns before to 7 ns after clock edge in 125 ps increments. This range may be shifted towards the positive region by 0 ns, 4 ns, or 8 ns.
Setup-and-hold Violation Recognizer Hold Time Range –
From 7 ns before to 8 ns after clock edge in 125 ps increments. This range may be shifted towards the positive region by 0 ns [+8, –8] ns, 4 ns [+12, –4] ns, or 8 ns [+16, 0] ns.
Trigger Position – Any data sample.
MagniVu Trigger Position –
MagniVu position can be set from 0% to 60% centered around the MagniVu trigger.
Storage Control (data qualification) –
Global (conditional), by state (start/stop), block, by trigger action, or transitional. Also force main prefill selection available.

Physical Characteristics

Dimensions	**mm**	**in.**
Height	262	10.3
Width	61	2.4
Depth	381	15
Weight	**kg**	**lb.**
Net	3.1	6.7
Shipping	6.3	13.7

▸ Ordering Information

TLA7Axx Logic Analyzer Modules

Includes: Probe retainer bracket, certificate of calibration, one-year warranty (return to Tektronix), and installation manual.

Probes must be ordered separately.

TLA7AA1 – 34 channel Logic Analyzer module, 8 GHz timing, 120 MHz state, 128 Kb depth (must select one probe option below). Options for up to 32 Mb depth and/or up to 450 MHz state.

TLA7AA2 – 68 channel Logic Analyzer module, 8 GHz timing, 120 MHz state, 128 Kb depth (must select one probe option below). Options for up to 32 Mb depth and/or up to 450 MHz state.

TLA7AA3 – 102 channel Logic Analyzer module, 8 GHz timing, 120 MHz state, 128 Kb depth (must select one probe option below). Options for up to 32 Mb depth and/or up to 450 MHz state.

TLA7AA4 – 136 channel Logic Analyzer module, 8 GHz timing, 120 MHz state, 128 Kb depth (must select one probe option below). Options for up to 32 Mb depth and/or up to 450 MHz state.

TLA7AB2 – 68 channel Logic Analyzer module, 8 GHz timing, 120 MHz state, 64 Mb depth (must select one probe option below). Option for up to 450 MHz state.

TLA7AB4 – 136 channel Logic Analyzer module, 8 GHz timing, 120 MHz state, 64 Mb depth (must select one probe option below). Option for up to 450 MHz state.

Logic Analyzer TLA7AAx Module Options

(Base configuration is 128 Kb depth at 120 MHz state.)

Opt 1S – Increase to 512 Kb Depth at 120 MHz State.

Opt 2S – Increase to 2 Mb Depth at 120 MHz State.

Opt 3S – Increase to 8 Mb Depth at 120 MHz State.

Opt 4S – Increase to 32 Mb Depth at 120 MHz State.

Opt 5S – Increase to 128 Kb Depth at 235 MHz State.

Opt 6S – Increase to 512 Kb Depth at 235 MHz State.

Opt 7S – Increase to 2 Mb Depth at 235 MHz State.

Opt 8S – Increase to 8 Mb Depth at 235 MHz State.

Opt 9S – Increase to 32 Mb Depth at 235 MHz State.

Opt AS – Increase to 128 Kb Depth lat 450 MHz State.

Opt BS – Increase to 512 Kb Depth at 450 MHz State.

Opt CS – Increase to 2 Mb Depth at 450 MHz State.

Opt DS – Increase to 8 Mb Depth at 450 MHz State.

Opt ES – Increase to 32 Mb Depth at 450 MHz State.

Logic Analyzer TLA7ABx Module Options

(Base configuration is 64 Mb depth at 120 MHz state.)

Opt. 1S – Increase to 64 Mb depth at 235 MHz state.

Opt. 2S – Increase to 64 Mb depth at 450 MHz state.

TLA Series Module Upgrades

You can increase the memory depth and state speed of most existing TLA Series logic analyzer modules. You can also install a TLA7Axx logic analyzer module into an existing TLA715/721/7XM/7012/7016 mainframe. Please refer to the TLA Family Upgrade Guide for further details.

Logic Analyzer Probe Selection Guidelines

A flexible choice of logic analyzer probes is available for use with TLA7Axx modules. Please see the logic analyzer probe data sheets for further information.

TLA7Axx Service Options

Opt. C3 – Calibration Service 3 Years.

Opt. C5 – Calibration Service 5 Years.

Opt. D1 – Calibration Data Report.

Opt. D3 – Calibration Data Report 3 Years (with Opt. C3).

Opt. D5 – Calibration Data Report 5 Years (with Opt. C5).

Opt. R3 – Repair Service 3 Years.

Opt. R5 – Repair Service 5 Years.

Opt. IN – Product Installation Service.

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www.tektronix.com

Product(s) are manufactured in ISO registered facilities.

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