BERTScope 17500A and BERTScope Si 17500C Signal Integrity Analyzers

BERTScope™ Si

Five Instruments in One:

- Pattern Generator
- Error Analyzer
- Stress Generator
- Sampling Scope
- Jitter Analyzer

- Full BERTScope Capabilities from 500 Mb/s to 17.5 Gb/s
- Pattern Generation, Error Detection and Advanced Signal Integrity Analysis for 16xFC
- Integrated Stress Generation to 17.5 Gb/s: SJ, RJ, BUJ, SSC, SI, and new F/2 jitter
- Jitter Map:
  - BER Based Jitter Decomposition – TJ, DJ, DDJ, ISI, DCD, BUJ, RJ, and more
  - Jitter Triangulation Enables Decomposition for PRBS-23, -31 and Packetized Live Data
- Automated FIR Tap Calculation for Pre-emphasis and Equalization
- Spread Spectrum Clocking (SSC) on data rates from 500 MHz to 17.5 GHz

The Vision of a Scope, the Confidence of a BERT, and Clock Recovery you can Count on.

SYNTHESYS RESEARCH, INC.

The Next Step

The BERTScope 17500A and BERTScope Si 17500C advance the BERTScope Family to 17.5 Gb/s and cover today's serial data interfaces from 1 Gb Ethernet (GbE) to 10 GbE and are designed to address future serial data interfaces including:

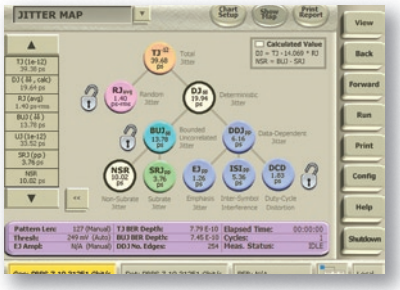
- 16x Fibre Channel
- 12 Gb/s SAS
- 8.0 GT/s Gen. 3 PCI Express®
- Potential 16.0 GT/s Gen. 4 PCI Express
- Proprietary chip interfaces
- Next Generation Backplanes

The BERTScope 17500A and Si 17500C reduce your time to market by providing the most advanced and comprehensive combination of signal integrity analysis and test tools available in a single instrument. They build on the existing capabilities of the BERTScope 7500 and 12500 families which include:

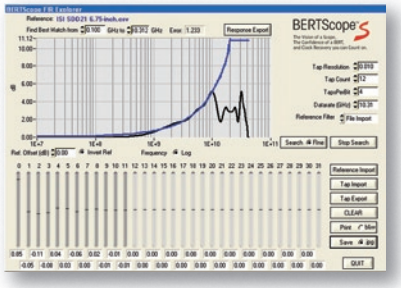
- BER analysis with patented error location analysis
- BER correlated eye diagram & mask testing
- MJSQ[1] compliant dual-Dirac based Jitter Peak analysis
- Q-Factor BER-based view of vertical eye opening
- BER contour analysis with contour compliance mask testing for compliance masks specified at deep BER levels
- Automated jitter tolerance compliance and margin testing

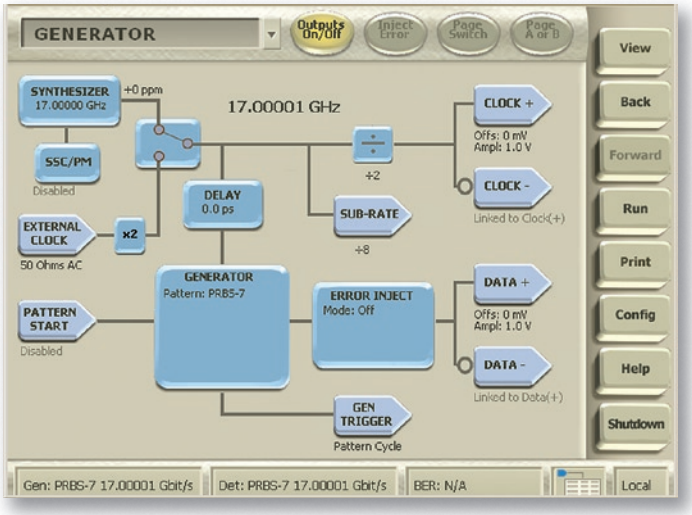
The BERTScope 17500A and Si 17500C add two major additional signal integrity analysis tools:

- Jitter Map, available as an option, performs jitter decomposition using BER based measurements, including on jitter separation on long patterns such as PRBS-31. More details on page 5.

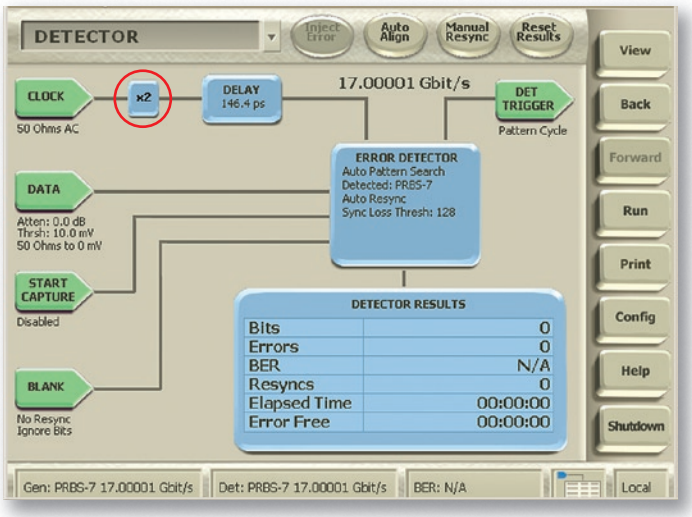


- FIR Explorer, easily converts insertion loss measurements into FIR tap settings for emulation or correction. See page 6.





The BERTScope 17500A and Si 17500C Pattern Generators provide data up to 17.5 Gb/s. Clock Outputs are ÷2 for synthesizer setting of 11.2 GHz and above.



The BSA 17500A and Si 17500C Error Detectors can use either full or half rate clocks by utilizing double data rate (DDR) clocking. DDR clocking uses both the rising and falling edges to clock the error detector. When using a clock supplied from the 17500A or Si 17500C Pattern Generator, DDR is used for data rates of 11.2 Gb/s and above. Select x2 (circled above) to use DDR clocking in the Error Detector.

1. Fibre Channel – Methodologies for Jitter and Signal Quality Specification – MJSQ, T11.2, Project 1316-DT, Rev 14, June 9, 2004

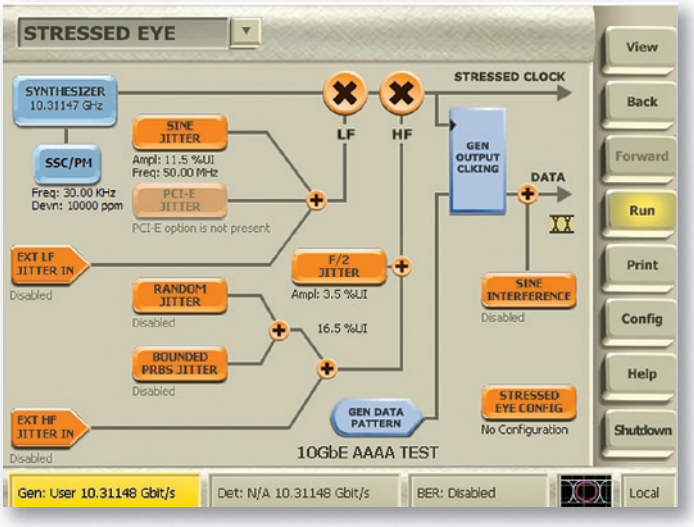
Enhanced Stress Generation

The BERTScope Si 17500C offers the standard stresses available in the BERTScope S extended to 17.5 Gb/s. It also features enhanced integrated stress generation:

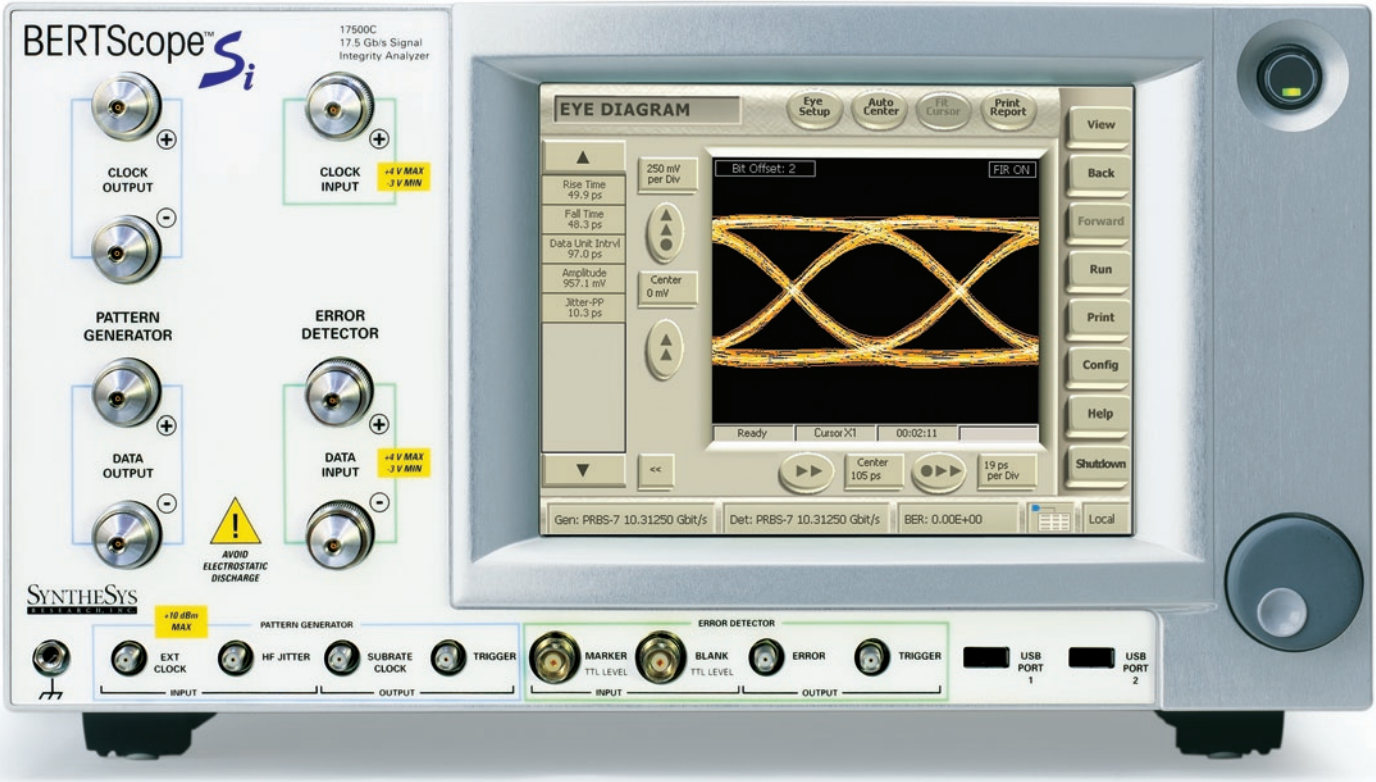
- F/2 jitter is available as an option for use in 10 GBASE-KR. F/2 jitter varies the pulse widths of odd vs. even bits in the data pattern (compared to conventional duty cycle distortion DCD which causes differences in pulse width between ones and zeroes).
- Second, Sinusoidal Jitter (SJ) amplitudes at jitter frequencies below 160 kHz have been greatly increased by phase modulating the Pattern Generator's clock source.

  Jitter tolerance SJ requirements met or exceeded include :

  - SONET - OC-192, OC-48, OC-12
  - SDH - STM-64, STM-16, STM-4
  - OTN – OTU 1, 2, 2e, 2f
  - Fibre Channel – 1x, 2x, 4x, 8x, 10x
  - Ethernet – 1GbE, XAUI, 10GBASE-R, 10GBASE-KR etc.
  - SATA and SAS through 6 Gb/s
  - PCI-Express® (PCIe)
  - OIF-CEI 6G, 11G
  - XFP MSA
- Spread Spectrum Clocking (SSC) on data rates from 500 MHz to 17.5 GHz
  - SSC range – SSC Modulation Calibrated from 20 - 40 kHz, uncalibrated to 160 kHz.
  - SSC can be used simultaneously with SJ and other stresses.



BERTScope Si 17500C stress generator selection page

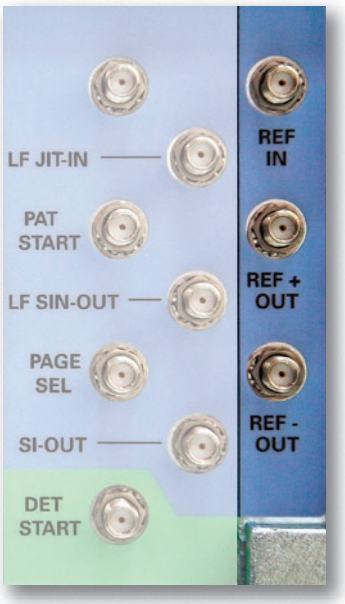


Sustained Evolution

The BERTScope 17500A and BERTScope Si 17500C also include other enhancements to the BERTScope Family:

- Rear panel differential reference clock outputs and single ended reference clock input at seven selectable frequencies; these may be used to phase lock a BERTScope to another BERTScope or other external instrument.
- Windows XP for better web security and compatibility with local IT policies.
- 128 Mb RAM memory enables the use and capture of extremely long stress patterns.
- USB port count increased from two to four.

The BERTScope 17500A and Si 17500C provide rear panel differential reference clock outputs and single ended reference clock input which can be used to phase lock to the BSA. The rear panel reference clocks frequencies are:



- 10 MHz
- 100 MHz
- 106.25 MHz
- 133.33 MHz
- 156.25 MHz
- 166.67 MHz
- 200 MHz

Jitter Map – BER Based Jitter Decomposition, Even for Long Patterns

Today's standards require jitter measurements that are often beyond the basic Total Jitter (TJ) separation into Deterministic Jitter (DJ) and Random Jitter (RJ). These new measurements can be found in both transmitter testing, where jitter must not exceed specified amounts, and in creating calibrated stressed eyes using a recipe of jitter types for receiver tolerance testing. Some examples include:

- Data Dependent Pulse Width Shrinkage (DDPWS) supports 8G Fibre Channel and SFP+ (SFF-8431)
- Uncorrelated Jitter (UJ) can be used for 8G Fibre Channel, SFP+, and IEEE 802.3aq (10GBASE-LRM) testing
- Non-ISI is used in DisplayPort
- DCD is included in Fibre Channel for data rates at 4G and below, is part of the stress recipe in SFP+, and is also used in OIF-CEI 2.0
- F/2 Jitter is implied in 10GBASE-KR and has appeared in drafts of 8 GT/s PCIe 3.0

All of these are available in the Jitter Map option.

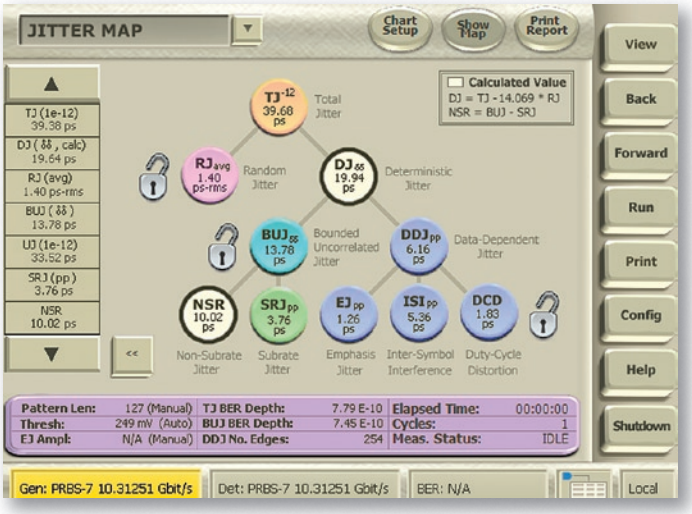
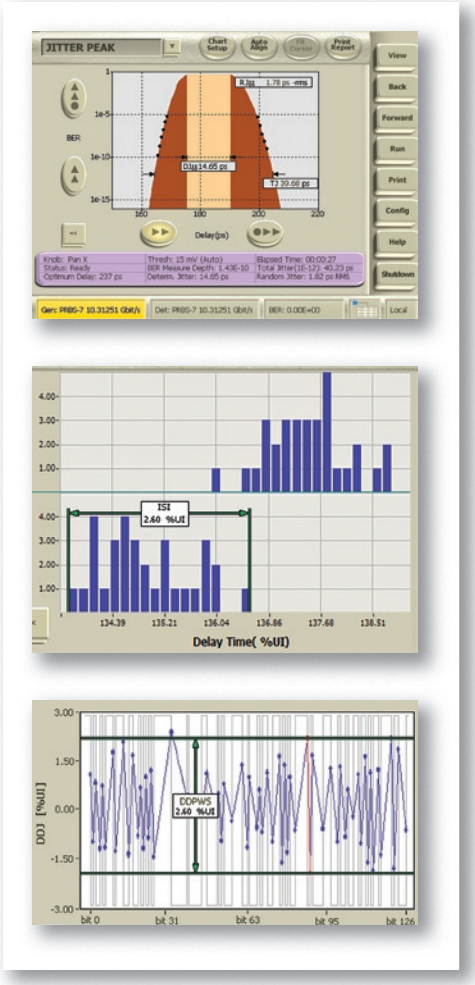


Figure 1. BERTScope Jitter Map provides detailed analysis of jitter components including: Random Jitter (RJ), Bounded Uncorrelated Jitter (BUJ), Sub-rate Jitter (SRJ), Deterministic Jitter (DJ), Data Dependant Jitter (DDJ), Inter-symbol Interference (ISI), Duty Cycle Distortion (DCD), and Emphasis Jitter (EJ).

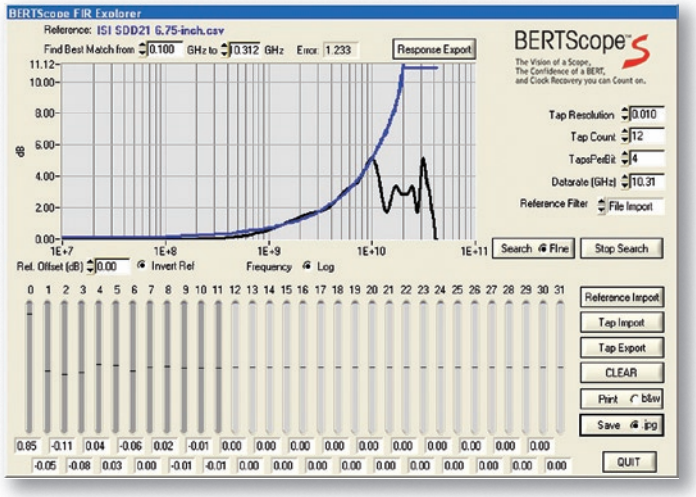


Get jitter answers fast with Jitter Map's intuitive UI. Use the "map" to navigate to detailed views of (top to bottom) Total Jitter using dual-Dirac, DDJ histograms, and DDJ per bit in the data pattern.

Key features of optional BERTScope Jitter Map include:

- The first instrument to provide deep BER based detailed jitter sub-component analysis. Jitter Map starts with the "gold standard" of deep BER measurement based dual-Dirac TJ and then leverages its ability to lock onto a data pattern in order to provide additional insight into jitter components.
- Jitter Map also enables detailed jitter decomposition on long data patterns (beyond PRBS-15) as well as active data traffic using Jitter Triangulation. This uses the acquisition of key jitter data from first running a short pattern, then locking down appropriate subcomponents. Long pattern analysis is suitable for the following standards:
  - PRBS-23 for future Gen 3 PCIe
  - PRBS-31 for SFP+, XFP, 10GbE, 40 GbE, 100GbE, & OIF-CEI
  - Live packetized data running up to 11.2 Gb/s (Live Data Analysis option required).

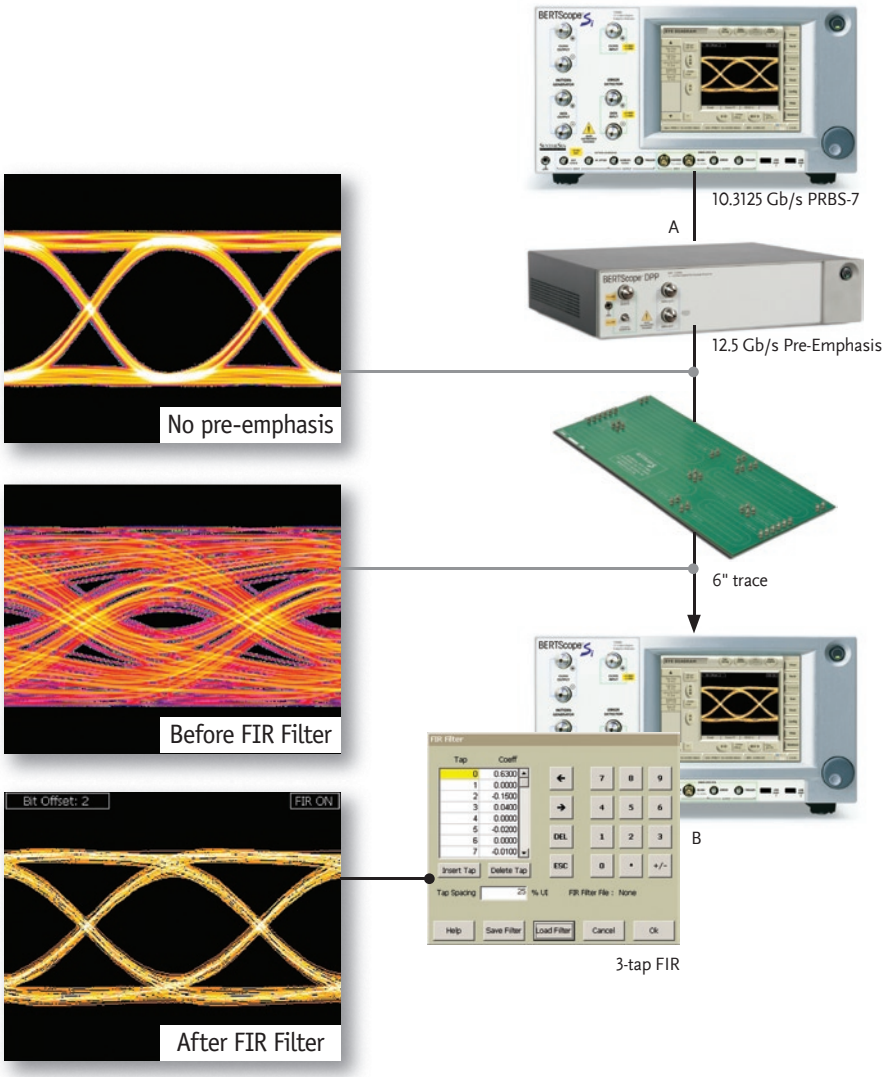
FIR Tap Optimization



In this example, the BERTScope FIR Explorer uses its 'Invert Ref' feature to determine 12 equalization tap values which yield a close match to the desired (blue) frequency response. This is needed to compensate for the frequency dependent loss of the 6.75 inch channel on the BERTScope ISI board at 10.3125 Gb/s.

BERTScope FIR Explorer is new software available from SyntheSys that has the following features:

- Works with customer-provided S21 channel data and suitable imported frequency responses.
- Uses a specified range of parameters including the number of taps and their spacing to search for a suitable matching fit to either the response (for channel emulation) or its inverse (for channel correction).
- Quickly open up closed eye diagrams.
- De-embed the effect of cables and adapters on the device under test.
- May be used with the BERTScope Digital Pre-Emphasis Processor (DPP) to optimize pre-emphasis tap values for patterns up to PRBS-31 and data rates up to 12.5 Gb/s.

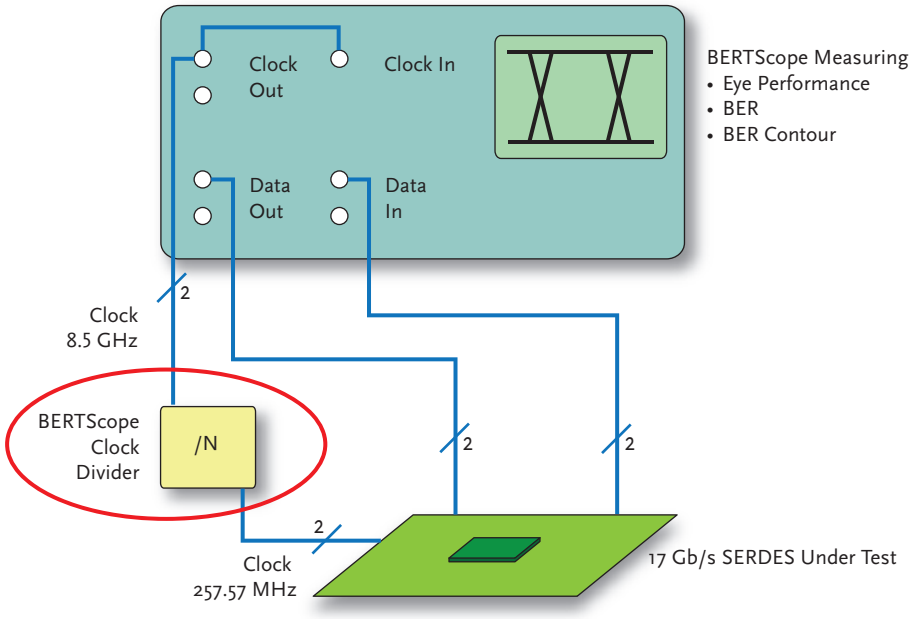


(Shown in CleanEye Mode)

The example shows how frequency response modification can be used to overcome channel loss, either through pre-emphasis (A), or equalization (B). Tap calculation can be applied to either end – the BERTScope DPP (A) provides up to 4 taps at one bit spacing, operational to 12.5 Gb/s and with long patterns such as PRBS-31. Receiver equalization emulation is available with BERTScope PatternVu (B) which provides an averaged waveform for analysis or export, at data rates to the maximum of the instrument model, to patterns up to PRBS-15, and with 30 taps of arbitrary spacing.

Working on 16x Fibre Channel?

In addition to BERTScope 17500A and Si 17500C integrated features, an optional external clock divider is available to supply additional subrate clocks to your Device Under Test (DUT). In this example of testing a 16xFC capable SERDES at 17 Gb/s, the BERTScope sends a half rate, 8.5 GHz clock to the available external BERTScope Clock Driver/Divider accessory which provides a divide by 33, 257.57 MHz subrate clock required by the 17 Gb/s SERDES. The BERTScope Error Detector is also triggered by the half rate clock and uses double data rate triggering to analyze the 17 Gb/s data stream coming from the SERDES.



BERTScope 12500A Clock Driver/Divider Accessory

Key Features:

- Divide-by-N (N from 1 to 256) Clock Outputs
- Usable to 12.5 Gb/s
- USB or Push Button Control of:
  - Divide ratios
  - Amplitudes
  - Offsets
- Usable with other instruments and equipment

BERTScope 17500 Family

BERTScope™

www.bertscope.com

BERTScope 17500A includes pattern generation, error detection, eye diagram analysis and Mask Testing. Additional options include:

- Physical layer analysis (BER contour, Jitter Peak, and Q Factor)
- Jitter Map
- Error Correction Coding and Mapping
- Live Data Analysis
- PatternVu Equalization Processing
- Rackmount
- 3 year extended warranty

BERTScope Si 17500C includes pattern generation, error detection, eye diagram analysis and Mask Testing, Physical Layer Analysis, Error Correction, Coding and Mapping. It also includes enhanced stress generation with added SJ range, SSC capability, as well as automated jitter tolerance testing. Additional options include:

- Jitter Map
- PatternVu Equalization Processing
- PCIe stress generation
- F/2 jitter generation
- Live Data Analysis
- Rackmount
- 3 year extended warranty

Related Literature

For more information on this and other products:

- BERTScope™ and BERTScope™ S Signal Integrity Analyzers Technical Specifications, SR-DS014
- BERTScope™ DPP Digital Pre-Emphasis Processor Product Brief SR-DS028
- BERTScope™ DCR; Digital Communications Receiver Product Brief SR-DS026
- BERTScope™ LTS Lightwave Test Set Product Brief SR-DS029
- BERTScope™ Differential ISI Board Product Brief, SR-DS018
- BERTScope™ CR Clock Recovery Instrument Product Brief, SR-DS016

Application information:

- Stressed Eye – Know what you are testing with, January 2006
- Evaluating Stress Components Using BER-Based Jitter Measurements, September 2005
- Combatting Closed Eyes: Pre-Emphasis and Equalization Basics, April 2008
- Telecom Jitter Analysis Using the BERTScope™ and BERTScope™ DCRj, January 2008
- Constructing a 10 GbE Optical Fibre Channel Stressed Eye, January 2006
- Testing the High Speed Electrical Specifications of an XFP Transceiver, July 2006
- Testing an SFP+ Transceiver to the 8+ Fibre Channel Specification, Part 1 & II, August 2008
- 10 GBASE-KR Compliance Testing, Rev. 1.1, December 2008

SYNTHESYS RESEARCH, INC.

3475-D Edison Way
Menlo Park, CA 94025 U.S.A.
Voice 650 364-1853
Fax 650 364-5716
info@synthesysresearch.com

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