Specifications

Output memory	
Waveform length (data and markers) Clock rate – Slow mode (10 Hz to 4 MHz) Clock rate– Fast mode (2 MHz to 100 MHz)	 24 to 16000000 in steps of one 24 to 16000000 in steps of four
Amplitude resolution of data words	selectable word length 8 bit to 14 bit; up to 16 bit at digital output
Marker channels Number	can be used as marker or trigger outputs (for word lengths up to 14 bit) 4
Multisegment waveform Segment changeover time without clock change with clock change	max. 30 segments 4 ms typ. 12 ms typ.
Clock generation	
Clock range	10 Hz to 100 MHz
Setting range	10 Hz to 105 MHz[1]
Resolution	1×10^{-7}
External clock input Clock rate	 10 Hz to 4 MHz (slow mode) 2 MHz to 100 MHz (fast mode)
Reference frequency	
Internal reference output Frequency Aging (after 30 days of operation) Temperature effect (0 °C to 45 °C) Level, rms Frequency adjustment	 10 MHz 1×10^{-5}/year $<2 \times 10^{-6}$/°C 0.5 V (into 50 Ω) electronic
External reference input Frequency Level, rms Input impedance	 10 MHz 0.1 V to 2 V 50 Ω
Signal output	
Outputs	I and Q[2]
Output impedance	50 Ω
Output voltage (V_p into 50 Ω) Fix mode Amplitude fine variation Resolution Level difference between the two channels Residual DC offset DC fine variation Resolution SFDR[3] (sinewave/clockrate) 1 MHz/10 MHz 5 MHz/50 MHz Variable mode Resolution Residual DC offset DC fine variation Resolution SFDR[3] (sinewave 1 MHz, clock rate 10 MHz)	 0.5 V, same for both channels ±10%, separately for each channel 0.01% <0.2% (at 1 kHz, after auto-alignment) <0.5 mV, 0.1 mV typ. (after auto-alignment) ±30 mV typ. 30 µV >70 dB, 80 dB typ. >60 dB, 75 dB typ. 0 V to 1 V, separately adjustable for each channel 3 digits <5 mV, 1 mV typ. (after auto-alignment) ±70 mV typ. 70 µV >50 dB (level >0.1 V), 70 dB typ. (level >0.5 V)
Skew between I and Q channel (filter off, clock rate 10 MHz, fix mode) Fine variation Resolution	 ±1 ns typ. <10 ps
Rise time	5 ns typ.

Adjacent-channel power	
WCDMA 3GPP FDD Test model 1 (64 DPCH channels) Offset 5 MHz Offset 10 MHz	 –78 dBc typ. –78 dBc typ.
Error vector	
IS-95 (QPSK)	0.35% typ. EVM (rms)
GSM (GMSK)	0.2° typ. phase error (rms)
DECT (2-FSK)	0.9% typ. FSK error
NADC, PHS (π/4DQPSK)	0.3% typ. EVM (rms)
Filters	
Operating modes	off (no filter), internal or external filter
Internal filters 25 MHz Freq. response Amplitude Group delay I/Q imbalance Amplitude Group delay Stopband attenuation 2.5 MHz Freq. response Amplitude Group delay I/Q imbalance Amplitude Group delay Stopband attenuation	 elliptic, 7th order + delay equalizer 0.15 dB typ. up to 25 MHz 500 ps typ. up to 20 MHz 0.05 dB typ. up to 25 MHz 200 ps typ. up to 20 MHz 70 dB from 75 MHz elliptic, 7th order + delay equalizer 0.15 dB typ. up to 2.5 MHz 5 ns typ. up to 2 MHz 0.05 dB typ. up to 2.5 MHz 1 ns typ. up to 2 MHz 70 dB from 7.5 MHz
External filters Impedance	one filter can be connected for each channel, BNC connectors on rear panel 50 Ω
Trigger	
CONT mode	repetitive output of loaded waveform after occurrence of trigger
SINGLE mode	single output of loaded waveform after occurrence of trigger
GATED mode	start of (repetitive) waveform output after occurrence of trigger until end of trigger event
Trigger signal	via remote control or trigger input
Trigger input Input level Max. permissible input voltage Pulse width (clock rate –slow mode) Pulse width (clock rate – fast mode) Delay between trigger input and output of first data word Slow mode Fast mode	BNC connector, selectable polarity TTL –0.5 V to 6 V min. 200 ns + 1 sample min. 11 samples 220 ns + (1 sample + 20 ns) jitter 21 samples + 1 sample jitter
Marker outputs	
Number of outputs	4, BNC connectors
Level	TTL, can be terminated into 50 Ω, (high >2 V)
BER measurement (option R&S AMIQ-B1)	
Data supplied by the DUT can be compared with a nominal random bit sequence; the results are transferred to the host computer (via the currently used remote control); the BER measurement can be controlled from R&S WinIQSIM™ and R&S SMIQ.	
Pseudo random bit sequences	2^9-1, $2^{11}-1$, $2^{15}-1$, $2^{16}-1$, $2^{20}-1$, $2^{21}-1$, $2^{23}-1$
Clock rate	max. 20 MHz

Clock source	each valid bit requires a clock, which is supplied by the DUT or the R&S AMIQ
Sync period	24 clocks
Interface Data Data enable Clock Restart	9-pin D-SUB connector, D-SUB BNC cable supplied in addition TTL TTL TTL TTL
Setup time	10 ns
Hold time	2 ns
Polarity	normal and inverted (data, clock, data enable)
Measurement time	selectable through max. number of data or error bits (max. 2^{31} bit), continuous measurement
Measurement results	BER in ppm (when set number of data or error bits is attained), not synchronized, no clock from DUT
Differential I/Q outputs (option R&S AMIQ-B2)[4]	
Provides the inverted $\overline{I}$ and $\overline{Q}$ signals and allows a DC voltage to be simultaneously superimposed on the output signal.	
Outputs	I, $\overline{I}$, Q and $\overline{Q}$
Operating mode	single/differential, selectable
Output impedance	50 Ω when on, 50 Ω or high Z when off
Bias voltage (EMF, to ground)	–2.5 V to +2.5 V (±10 mV) for both I and Q channels separate, common setting for I and $\overline{I}$ or Q and $\overline{Q}$
Resolution	<1.5 mV
Difference between I and $\overline{I}$ or Q and $\overline{Q}$	<0.5% + 1.5 mV
Output voltage (differential EMF between the I and $\overline{I}$ or Q and $\overline{Q}$ outputs, unless otherwise specified, V_p)	
Fix mode Level difference I ↔ Q I ↔ $\overline{I}$ (Q ↔ $\overline{Q}$) Residual DC offset DC fine variation Resolution	2 V, same for both I and Q channels <0.5% (at 1 kHz, after auto-alignment) <0.5% (at 1 kHz, after auto-alignment) <1 mV (to ground, after auto-alignment) ±120 mV typ. 120 µV
Variable mode	0 V to 4 V, separately adjustable for I and Q channels
Resolution DC fine variation Resolution	3 digits ±280 mV typ. 280 µV
Digital I/Q output (option R&S AMIQ-B3)	
Output	68-pin SCSI connector (mini D-SUB, half pitch)
Channels	I and Q
Resolution	8 bit to 16 bit (selectable, no marker output for word lengths >14 bit)
Max. clock frequency	100 MHz (if an external clock is used, the internal delay time from 20 ns to 25 ns between the input clock and the output data has to be taken into account above 40 MHz)
Output impedance	30 Ω to 50 Ω typ., high impedance with low level at pin 66
Output level	LVT or ABT level (data, marker and clock); the high level of the data, marker and clock signals is automatically adapted to the selected supply voltage for external circuits
V_{cc} output	+3.3 V or +5 V
Remote control and memory	via IEC 60625 (IEEE 488) and RS-232-C
Command set	SCPI 1996.0 with extensions
IEC/IEEE interface functions	SH1, AH1, T6, L4, SR1, RL1, PP1, DC1, DT1, C0
Mass memory	floppy disk drive (3.5", 1.44 MB), hard disk 8 GB
Download time (4 000 000 I/Q samples from built-in hard disk)	27 s
General data	
Operating temperature range	+5 °C to +45 °C; meets EN 60068-2-1, Edition: 1995-03 and EN 60068-2-2, Edition: 1994-08
Storage temperature range	–20 °C to +60 °C
Damp heat	80% relative humidity at +30 °C
Vibration, sinusoidal	5 Hz to 150 Hz, max. 2 g at 55 Hz, 0.5 g const. 55 Hz to 150 Hz, meets EN 60068-2-6, Edition: 1996-05, EN 61010-1 and MIL-T-28800D class 5
Electromagnetic compatibility	meets EN 61000-6-3 and EN 61000-6-4 (EMC Directive of EU)
Immunity to RFI	10 V/m
Power supply	100 V to 120 V ± 10%, 50 Hz to 400 Hz, 200 V to 240 V ± 10%, 50 Hz to 60 Hz, autoranging, 150 VA
Safety	meets EN 61010-1, Edition: 1994-03 CAN/CSA-C22.2 No. 1010.1-92 UL Std. No. 3111-1
Dimensions (W × H × D)	427 mm × 88 mm × 450 mm
Weight	8.7 kg

[1] Specs at clock >100 MHz not guaranteed, max. ambient temperature +35 °C.

[2] $\overline{I}$ and $\overline{Q}$ in addition when option R&S AMIQ-B2 is used.

[3] Spurious-free dynamic range.

[4] All data not specified here are identical to those of the R&S AMIQ without option R&S AMIQ-B2 (I and Q only).