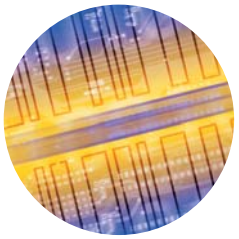
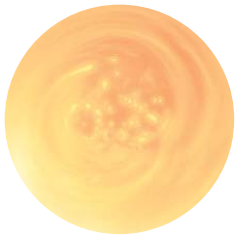
Agilent N4901B / N4902B

Serial BERT

13.5 Gbps
7 Gbps

Product Overview





Your Flexible High-Performance Solution

Agilent Technologies

Pattern

PRBS:

2^n-1 for n = 7, 10, 11, 15, 23, 31

Zero Substitution:

2^n for n = 7, 10, 11, 13, 15, 23

Variable Mark Density:

1/8, ¼, ½, ¾, 7/8 at 2^n for n = 7, 10, 11, 13, 15, 23

User-programmable Patterns:

variable length from 1 bit to 33,554,432 bits (2^{25})

Pattern Generation

Range of operation:
620 Mbps - 13.5 Gbps (external clock)
620 Mbps - 13.5 Gbps (internal clock)

Ampl.: 0.1 Vpp - 1.8 Vpp

Offset: -2 V to 3 V

Transition Times: <25 ps (10-90%)

Jitter: 9 ps pp typical

Delay Control Input: ±100 ps DC to 1 GHz <10.5 Gbps

Error Detector

Range of operation:
620 Mbps - 13.5 Gbps (external clock)
620 Mbps - 13.5 Gbps (internal clock)

Max Ampl.: 2.0 Vpp

Sensitivity: 50 mV

Decision Threshold: -2 V to 3 V

Clock/Data delay: ± 1.612 ns

CDR ranges:
(9.90 - 10.9) Gbps BW 6.0 MHz typ.
(4.23 - 6.40) Gbps BW 3.6 MHz typ.
(2.12 - 3.20) Gbps BW 1.8 MHz typ.

Connectivity

LAN
USB
GPIB
Parallel/serial/USB ports for connecting various peripherals

Online help

The on-line help system is a complete operating manual and software reference

Easy setup of the powerful Pattern Generator...

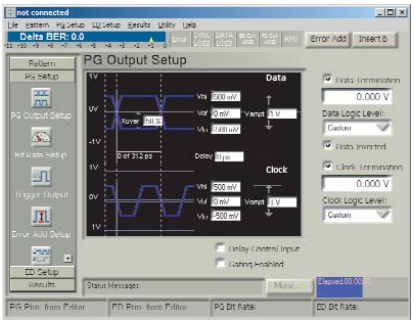


Figure 1: Pattern Generator Setup

The Serial BERTs offer the most flexible and powerful pattern, data and clock generation from 620 Mbps up to 13.5 Gbps or 7 Gbps. Capabilities such as Jitter Modulation, differential signalling including LVDS, divided clock generation in combination with its superior pulse performance and industry-leading waveform quality makes the Serial BERTs even more valuable for addressing a broad-range of applications and covering your specific test need!

...and Error Detector

The Serial BERTs Error Detector provides the critical gear for fast and in-depth problem analysis. With industry-first, leading edge capabilities such as integrated Clock Data Recovery (CDR), true differential data analysis including LVDS and low input sensitivity, the new Serial BERTs allows you to address a wide range of applications and technologies.

Figure 4: N4901B SerialBERT

The easy-to-use and intuitive user interface allows you to setup your test parameters quickly and efficiently, no matter if you are sitting in front of a touch screen or working remotely by using a LAN, USB or GPIB connection! With many pre-defined settings available, the most commonly used test parameters (e.g. common data logic levels such as LVDS, ECL, PECL) are available at the touch of a button. Custom settings are available by simply changing respective parameters, which can be saved onto the instrument for future use.

Figure 2: Easy to use

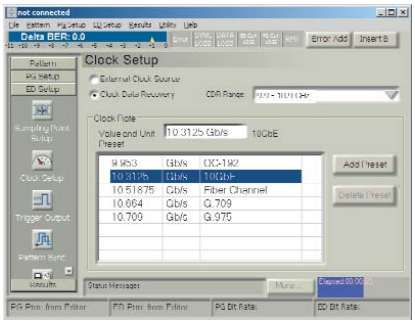


Figure 3: Serial BERT Error Detector

In combination with the comprehensive software and measurement suite, the Serial BERTs make your test even more efficient and reliable. Both the open Windows XP operating system and the expandable software and measurement suite accommodate upcoming test needs, applications and technologies by simply adding new software pieces.

Superior performance...

- Frequency agile operation range
- Fast transition times
- Low intrinsic jitter
- True differential data generation/analysis
- Industry-leading waveform generation
- Jitter modulation capabilities
- Flexible voltage levels incl. LVDS

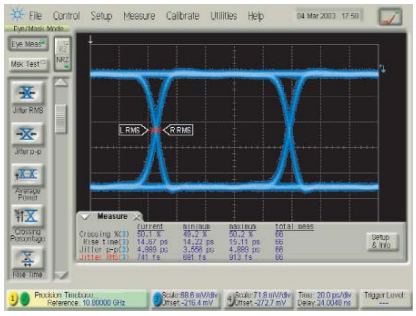


Figure 5: Superior Waveform

... comprehensive analysis capabilities...

- Bit Error Ratio measurements
- Jitter PP, RMS, RJ/DJ
- Spectral Decomposition of Jitter
- Bathtub incl. setup and hold time
- Q-factor
- Eye contour
- Fast Eye Mask

...and double design power...

Figure 6: Agilent 86100C Infiniium DCA-J

combined with

Figure 7: Agilent N4901B Serial BERT

...equals the complete test picture!!

Advantages for R&D and Manufacturing

- Lowers overall cost of test through:
  - o Addressing a wide range of applications and technologies
  - o True differential data generation and analysis
  - o Jitter modulation capabilities
  - o Integrated CDR at around 3 Gbps, 6 Gbps and 10 Gbps
  - o Code compatibility with the 71612C and 86130A
  - o Superior waveform quality
  - o Unique measurement and analysis capabilities

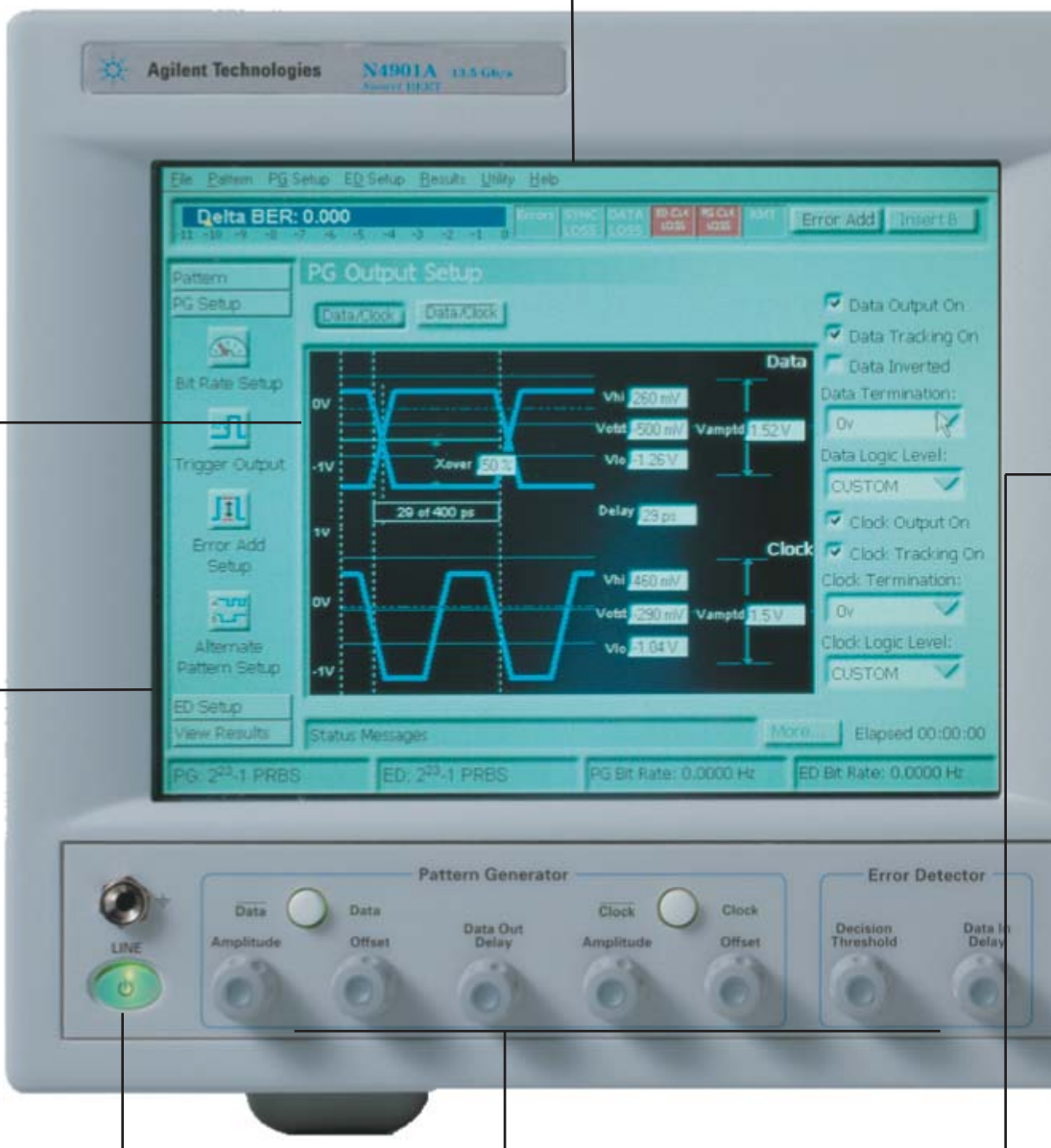
- Flexible I/Os useful for a wide range of applications:
  - o External Clock In - allows to insert external clock signals
  - o Trigger Out - outputs divided clock signals or trigger signals
  - o Delay Control In - allows Jitter modulation
  - o AUX Out - provides extracted clock (CDR) or data stream
  - o 10 MHz Ref IN - keeps other instruments in sync

- Software and Measurement Suite:
  - o Provides sophisticated measurements for device characterization in R&D (e.g. bathtub curve with RJ/DJ Separation, Spectral Decomposition of Jitter, Q-factor)
  - o Allows to define pass/fail criteria for manufacturing test (e.g. Fast Eye Mask, Bathtub curve)

- Ease-of-use concept:
  - o Intuitive touch screen user interface
  - o Open Win XP software platform
  - o Pre-defined settings for all common parameters
  - o Save your custom settings just like any other document on your PC
  - o Download new software pieces directly from the internet
  - o Remote controllable via LAN, USB and GPIB
  - o Remote programmable via HP VEE, Labview, C / C++.

Serial BERT: *In Detail*

Status Bar
Provides key status information while performing critical measurements



Graphical Status
Allows easy control of your measurement setup

Touchscreen User Interface
Allows the instrument to be controlled without any external devices

On/Off

Easy-Access
Allows access to frequently used parameter values

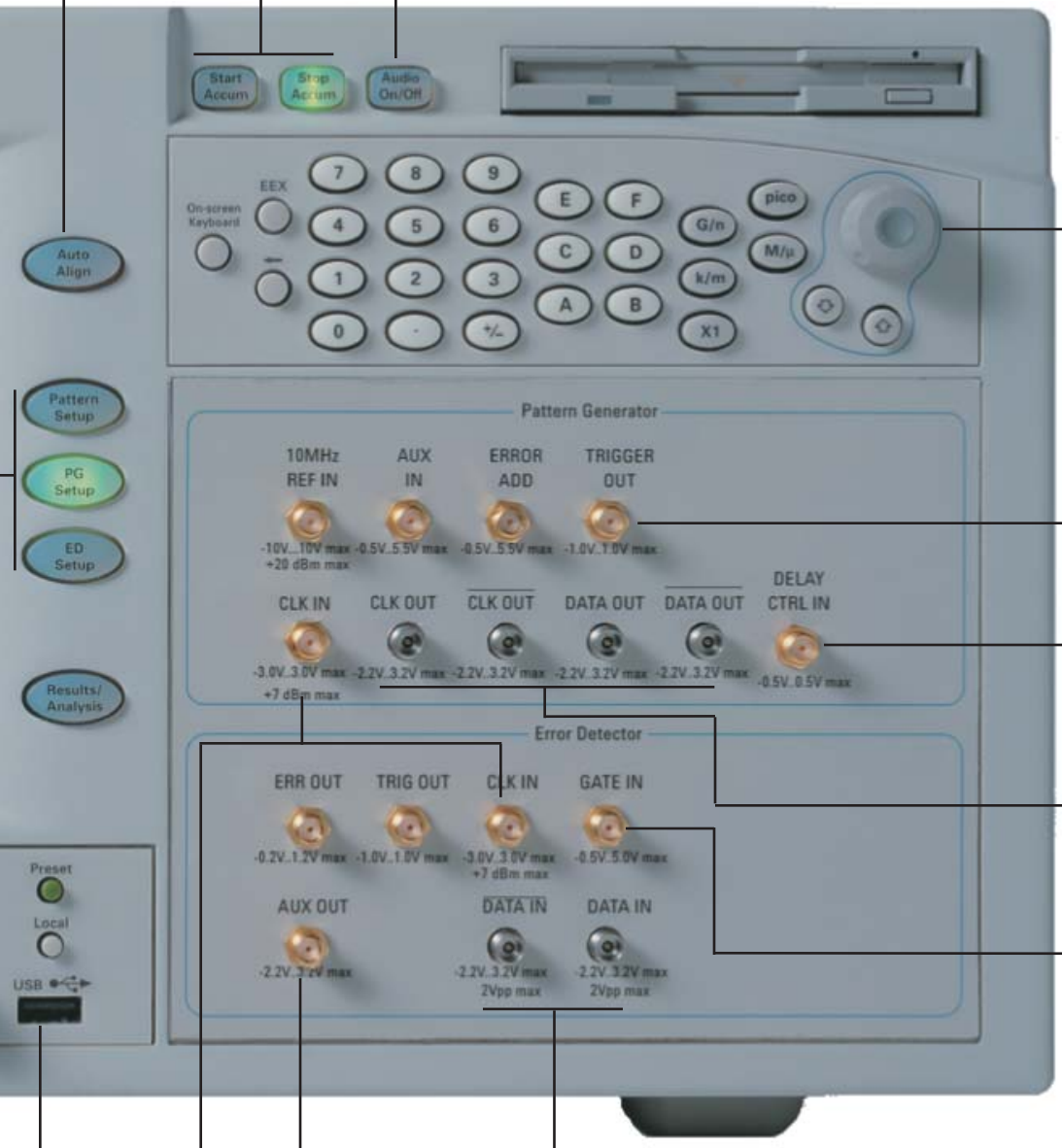
One-Touch User Interface Control

Front-side USB Port
Allows various peripherals to be connected to the Serial BERT

Start/Stop
Allows to start setup measurements

Auto Align
Finds optimal sample point

Audio
Provides acoustic signals



Selector Knob
Alters the parameters selected on screen

Trigger Out
Provides Trigger Signals and Divided Clock Signals

Delay Control In
Allows "Jitter" to be added on Data with up to 200 ps delay and DC to 1 GHz

Diff. Data and Clock Out
Provides leading-edge signal performance from 620 Mbps - 13.5 Gbps

Gate In
Allows gating signals to be inserted

AUX Out
Allows recovered clock signals to be output

Differential Data In
Allows data to be analyzed on differential channels

Clock In
Allows the Pattern Generator to work with an external clock source. Also allows the Error Detector to be connected to any clock source, whether internal or external

Figure 8: Serial BERT in detail

Software and Measurement Suite

The Software and Measurement Suite of the Serial BERT 13.5 Gbps and 7 Gbps offers comprehensive analysis features for in-depth insight for design verification and efficient pass/fail testing for manufacturing.

Besides comprehensive BER measurements, the following applications are especially suitable for design verification/R&D providing critical analysis gear for testing your device under test.

- Spectral Decomposition of Jitter
- Output Timing incl. RJ/DJ Separation and Setup/Hold time,
- Output Level Measurement
- Eye Contour

provide critical analysis gear for verifying your device under test.

For manufacturing test, pass/fail criteria are custom selectable for all measurements in order to perform fast end efficient go/no-go testing. The powerful Fast Eye Mask measurement with up to 32 user-defined points is especially suitable for manufacturing test.

Eye Contour

For device characterization, the eye opening measurement generates a three-dimensional bit error rate (BER) diagram as a function of the sample delay and the sample threshold. Besides the eye opening, the eye contour measurement provides results for the optimum sample point. The eye opening measurement allows you to select different views such as eye contour, pseudo color and equal BER plots.

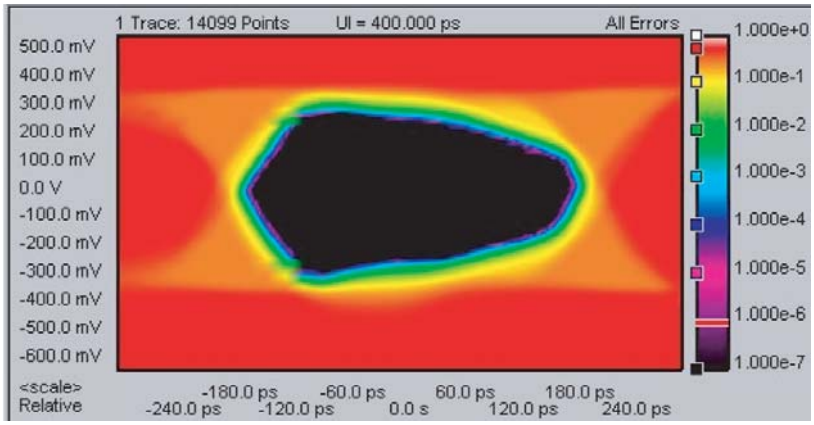


Figure 9: Eye contour

Spectral Decomposition of Jitter

This measurement provides a technique for the Spectral Decomposition of Jitter components, which helps debugging as well as design verification and characterization of devices. This measurement hooks up on the RJ/DJ Separation provided by the Output Timing Measurement.
The decomposition technique allows inband and outband characterization of circuits and devices including PLLs and CDRs.
This measurement helps to separate even the smallest amounts of periodic jitter (for example) from the random jitter floor providing top frequency/power spots as well as Total Power and Noise Power.

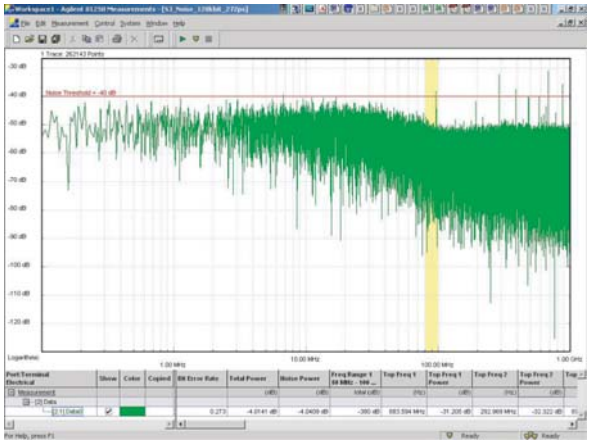


Figure 10: Spectral Decomposition of Jitter

Output Timing Measurement

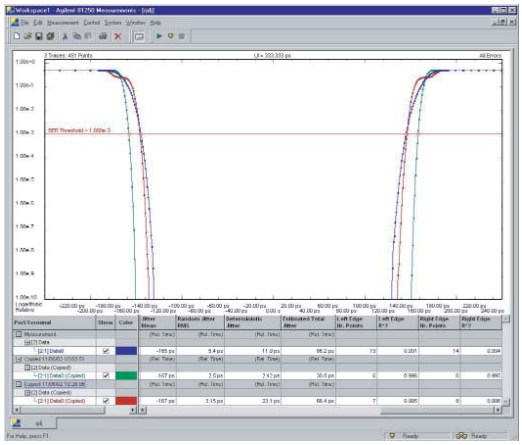


Figure 11: Output Timing Measurement

This measurement measures the BER of the DUT´s output versus sample point delay, which is graphically displayed as bathtub curve. Available results are setup/hold time, phase margin and Jitter incl. total jitter (rms, peak-to-peak) RJ/DJ Separation. The Output Timing measurement is available as bathtub plot and as a histogram.

Output Level Measurement

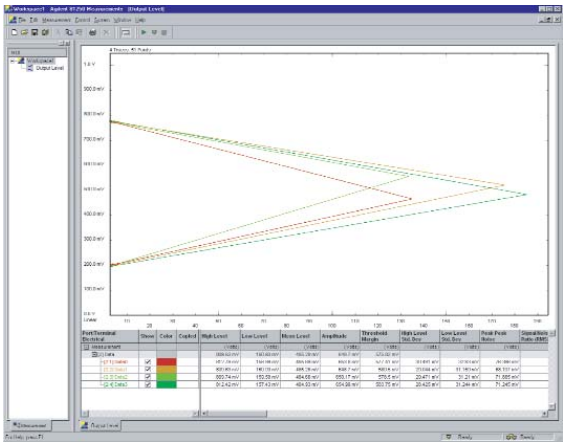


Figure 12: Output Level Measurement

The method used by this measurement is commonly known as Variable Decision Threshold Method. It provides a "vertical" analysis of the eye opening seen by the receiver. The Output Level measurement provides also Q-factor results, which are describing the quality of the received signal. The Output Level Measurement allows selecting views for BER vs. threshold, BER Histogram vs. threshold and Q from BER vs. threshold.

Fast Eye Mask Measurement

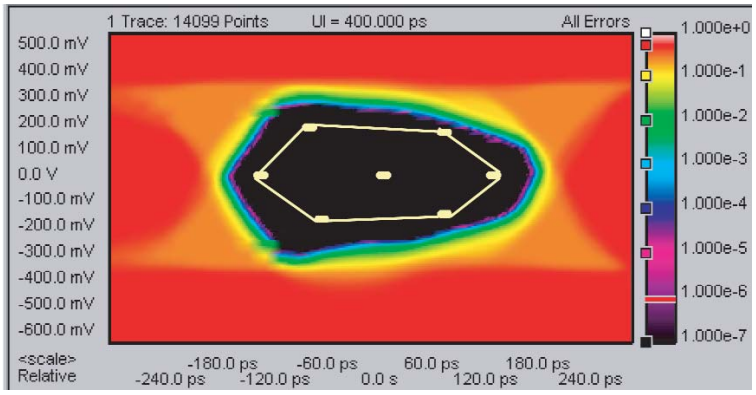


Figure 13: Fast Eye Mask Measurement

The fast eye mask measurement is ideal for use in manufacturing as a measurement typically takes just one second (including synchronization). This measurement records the BER of a pre-defined number of points (1 to 32 defined by a threshold and timing value relative to the starting point of the measurement. You enter the pass/fail criteria of the measurement and the BER threshold, find the middle point of the eye and then run the BER.

Related Literature	Pub. No.
• N4901B SerialBERT 13.5 Gbps Datasheet	5988-9674EN
• N4902B SerialBERT 7 Gbps Datasheet	5988-9675EN
• N4901B SerialBERT Product Note	5988-9676EN
• Physical Layer Test Brochure	5982-9514EN

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