# Agilent ParBERT 81250

## Parallel Bit Error Ratio Tester

Product Overview

Version 5.1 (Corresponds to ParBERT 81250 Software revision 5.1)


**The Only Parallel Bit Error Ratio Solution for testing at 675 Mbit/s, 1.65 Gbit/s, 2.7 Gbit/s, 3.35 Gbit/s, 10.8 Gbit/s, 13.5 Gbit/s and 45 Gbit/s**


Agilent Technologies

# Agilent ParBERT 81250

**Agilent ParBERT 81250 is a modular parallel electrical and optical bit error ratio (BER) test platform, which works up to 45 Gbit/s. The ParBERT 81250 platform comprises modules that work at 675 Mbit/s, 1.65 Gbit/s, 2.7 Gbit/s, 3.35 Gbit/s, 10.8 Gbit/s and 45 Gbit/s. The system generates pseudo random word sequences (PRWS), standard pseudo random binary sequences (PRBS) and user-defined patterns on parallel lines. You can analyze bit error ratios with user-defined patterns, PRBS/PRWS or mixed data (a combination of user-defined patterns and PRBS).**

ParBERT 81250 is a perfect fit for parallel-to-serial, serial-to-parallel, serial-to-serial and multiple serial BER test. Examples comprise multiplexer and demultiplexer (Mux/Demux) - or SerDes (serializer/deserializer) - testing used in telecom and storage area network (SAN) ICs, multiple transmitter and receiver testing in manufacturing, amplifiers as well as 10GbE and forward error correction (FEC) device testing.

ParBERT 81250 also provides data and control signals for the DUT if required.

**The ParBERT Software Suite is a ready-to-use package, which offers different levels of measurement analysis:**

**1.** Fast pass/fail measurements ideal for production
**2.** Output Timing measurements provide results for setup & hold times, skew between channels, phase margins, detailed Jitter results (RJ/DJ/TJ), and eye opening specification results
**3.** Output level measurements provide results for high/low levels, amplitudes, threshold margins and Q-factor analysis
**4.** Graphical results for detailed root cause analysis - see trends clearly and fast, e.g. color and contour plots

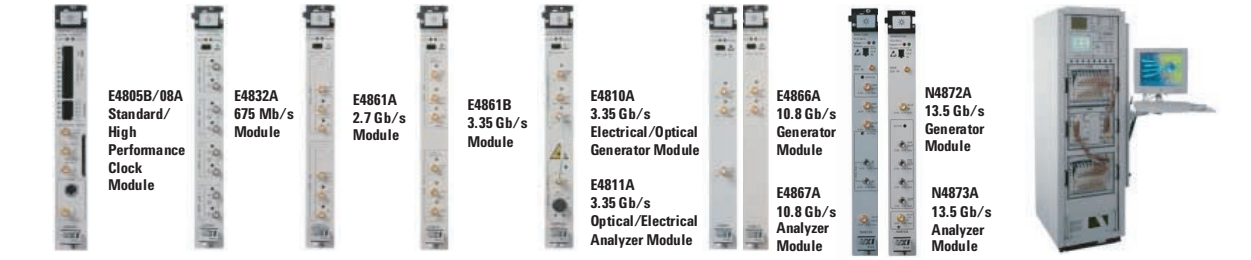
**Agilent ParBERT 81250 is particularly suitable for the following applications:**

**1.** 10GbE device testing
**2.** Multiplexer and Demultiplexer Test
- OC-768 device testing: You can test 16:1 and 4:1 40G devices using the ParBERT 81250 45G and either 3.3 Gbit/s or 10.8 Gbit/s modules
- OC-192 device testing: The ParBERT 81250 10.8 Gbit/s modules enable testing of the serial high-speed side of Muxes/DeMuxes. Combined with 675Mbit/s, 1.6Gbit/s, 2.7Gbit/s or 3.3 Gbit/s modules you can test both sides of multiplexers/demultiplexers
- OC-48 device testing

**3.** Characterization of SAN ICs
**4.** Manufacturing Test of multiple Transmitters, Receivers, Transceivers and Amplifiers
**5.** FEC Device Test

**For more information on these applications, please see brochure p/n 5968-9250E. For information on the Agilent ParBERT 81250 45 Gbit/s, please see p/n 5988-3020EN. For more information on ParBERT 3.35 Gbit/s optical/electrical mod-ules, please see p/n 5988-5901EN. This document focuses on the ParBERT platform up to 10.8 Gbit/s.**

## Modules




## Front Ends

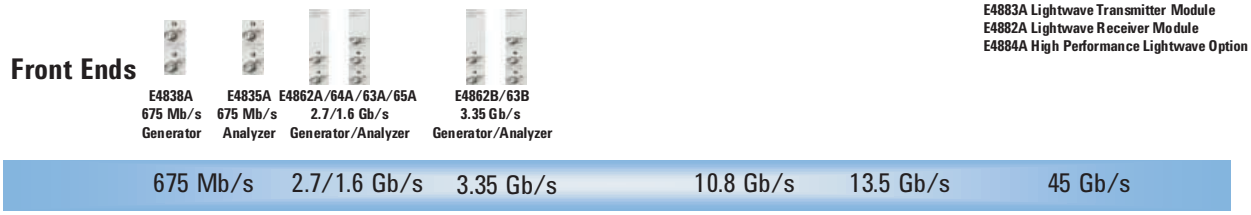



**Figure 1: ParBERT Product Family**

## ParBERT 81250 Key Features & Benefits

| Features | Benefits |
|---|---|
| Modular, flexible and scalable platform architecture<br>· Up to 128 channels @ 675 Mbit/s<br>· Up to 64 channels @ 3.35 Gbit/s, 2.7 Gbit/s<br>· Up to 30 channels @13.5 Gbit/s, 10.8 Gbit/s | · Grows with customer's test and application needs<br>· Covers a wide range of technologies and applications |
| Generator and Analyzer modules available from 675 Mbit/s up to 45 Gbit/s | Allows the configuration of a system to fit the customer's application needs |
| Mix of channels (generator/analyzer) and speed classes | Provides unique flexibility to test complex devices with many channels and/or frequencies, e.g. Serial bus applications, Mux/Demux (SerDes), FEC |
| Generate pseudo random word sequences (PRWS) and standard PRBS up to $2^{31}$-1; Analyze bit error ratios with user-defined data, PRBS or mixed data from parallel ports | Perform parallel BER measurements - ideal for Mux/Demux applications |
| Generate and analyze single-ended, low voltage and differential signals - including true differential | · Test logic technologies e.g. LVDS, ECL, PECL, SSTL-2<br>· Generate the necessary signals to perform margin tests, emulate frequency and level changes and stress your device as far as possible |
| Data generation and analysis with sequencing and looping | · Generate complex sequences that contain memory-based (up to 32Mbit) and/or PRBS/PRWS data<br>· Generate data packets with header and payload<br>· React to control signals from the DUT |
| Auto phase & auto delay alignment | · Auto alignment of expected data with incoming data<br>· Save time as you do not need to find the correct sample point manually - typically takes just 100ms, so ideal for manufacturing |
| Each generator or analyzer channel has independent programmable control of voltage levels and timing delay | Allows device characterization for a wide range of technologies/applications in the semiconductor and communication industry |
| Interrupt-free change of analyzer delay/generator delay (13.5 Gbit/s and 3.35 Gbit/s; other speed classes generator only) | Continuous running signals for measurements where changing analyzer delay is necessary |
| Jitter modulation (13.5 Gbit/s and 3.35 Gbit/s) | Allows jitter tolerance testing to be performed |
| Variable Cross (13.5 Gbit/s and 3.35 Gbit/s) | Provides real-world stress |
| Windows® 2000/NT 4.0 based user software | Provide "standard" and "detailed" views for performing measurements fast and efficiently |
| Plug and play drivers | Allows remote access and simplifies remote program development |
| Measurements Suite | · DUT output timing measurement - bathtub curve with jitter analysis (RJ/DJ separation), skew between channels, setup and hold times<br>· Output level measurement - amplitude information, high/low level and Q-factor<br>· Eye opening measurement - color and contour plots<br>· Fast eye mask measurement - automatic threshold adjust, fast and efficient insights for manufacturing test<br>· Comprehensive BER measurement - actual and accumulated BER, errors of ones and zeros, total bits transferred and file capturing for post-processing analysis. |

# Key Features (continued)

## Perform Parallel BER measurements up to 13.5 Gbit/s

ParBERT 81250 makes testing of Mux/Demux (serializer/deserializer) devices easier. Only ParBERT 81250 is able to generate pseudo-random-word sequences (PRWS) on the parallel side and analyze bit-error-ratios with user-defined patterns, PRBS up to $2^{31}$-1 or both combined.

## PRBS/PRWS and memory capability

The polynomial $2^n$-1, the PRBS algorithm and the parallel bus width define PRWS. The bits of the PRWS are assigned to parallel lines and are then multiplexed to form a PRBS (see figure 3).

## Auto phase and auto delay alignment

As the latency from the input to the output is often not known exactly, or it is not deterministic, synchronization between incoming data and outcoming data has to be carried out. ParBERT 81250 has three capabilities to synchronize/align the incoming data automatically (see figures 4 and 5):

1) Data shift bit-by-bit if PRBS is used

2) Detect Word if user-defined patterns are used

3) Moving of the sampling point delay of the analyzer up to 10ns without stopping the instrument. Moving of the sampling point delay can also be used in addition to the alignment of data patterns (1 and 2) to refine the synchronization.

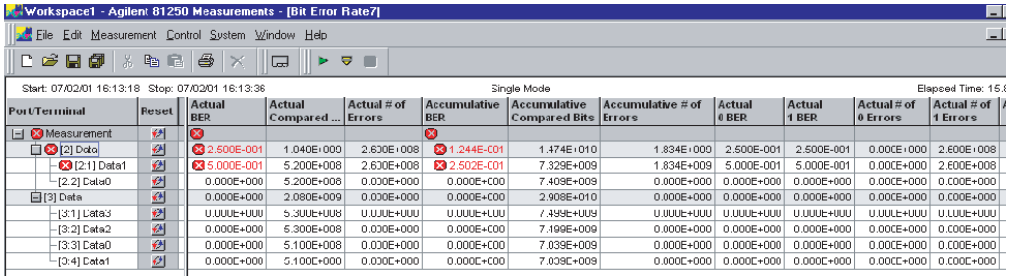



**Figure 2: BER results screen**

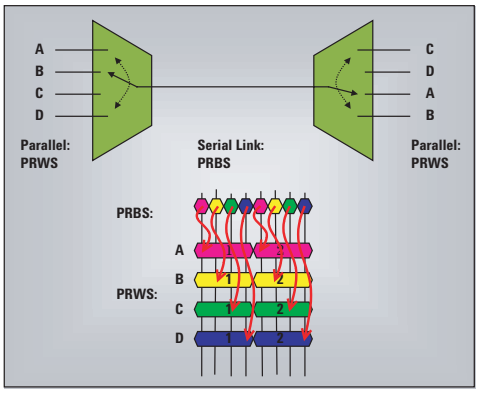



**Figure 3: MUX/DEMUX Application: Relationship between PRBS and PRWS**

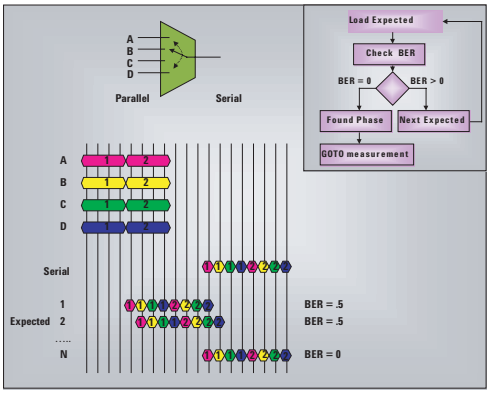



**Figure 4: Mechanism of auto-phase and auto-delay assignment**

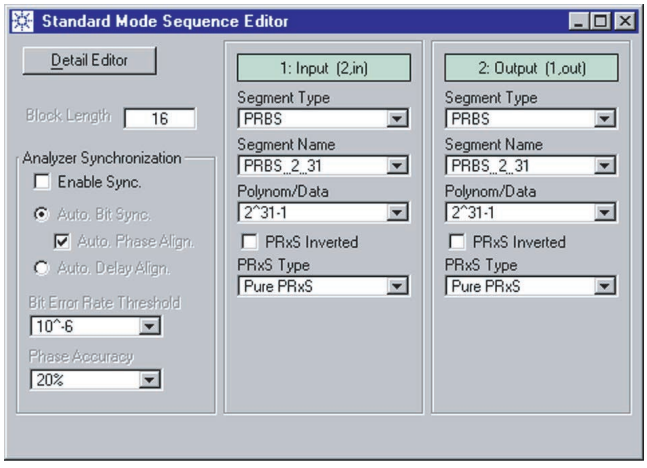



**Figure 5: Standard view when choosing PRBS/PRWS patterns and data synchronization mode**

## Interrupt-free change of analyzer delay

The analyzer delay can be changed ±1 period whilst the instrument is running without causing it to stop see figure 6. The 13.5 Gbit/s and 3.35 Gbit/s modules can do this on the Analyzer and Generator.

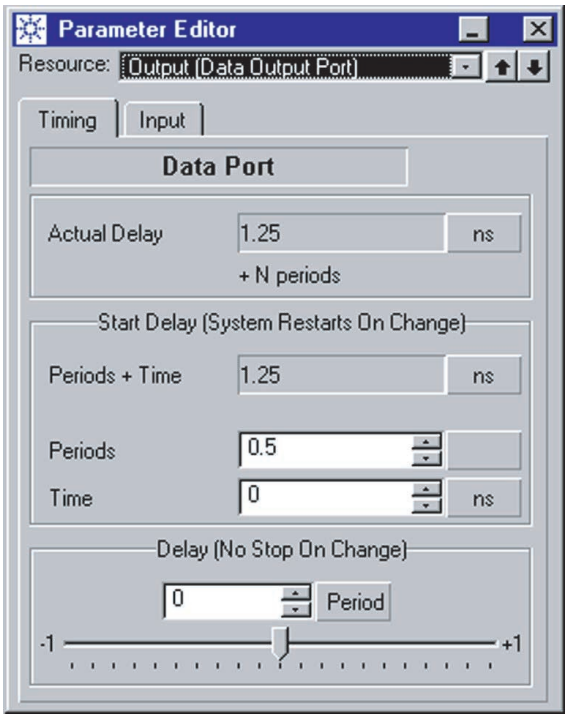



**Figure 6: Parameter Editor for analyzer timing**

## Multiple frequencies

The modular architecture of ParBERT allows the use of different channels at different speeds. Therefore it is possible to combine channels of different speed classes in one ParBERT system. A ParBERT system can be configured with one or more clock groups. Each clock group is controlled from one clock module. Within one clock group (one clock module controls a group of channels) a frequency ratio of $2^n$, n =1,2,....10 is possible, see figure 7.

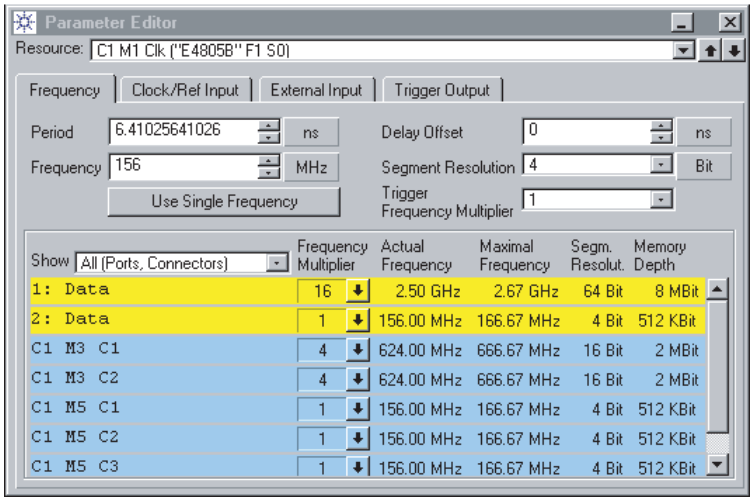



**Figure 7: Parameter Editor for setting multiple frequencies in one system**

With the two clock groups any frequency ratio m/n, n=1,2,...,256 is possible. The 'application examples' show some 'two-clock-system' configurations

# Fundamental Platform Description

The idea of the ParBERT 81250 product structure is that you receive the instrument, which meets your measurement needs exactly. The ParBERT modularity offers modules and frontends. At 13.5 Gbit/s and 10.8 Gbit/s there are dedicated modules for Generators and Analyzers. At 3.35 Gbit/s, 2.7 Gbit/s, 1.6 Gbit/s and 675 Mbit/s the modules carry 2/4 front-ends. The **front-ends** determine which kind of output or input connectors your specific instrument has. This means front-ends determine the speed and input/output capabilities of your instrument. A mix of front-ends is possible within the modules. The front-ends are placed in **data modules,** which are responsible for sequencing, generating and analysing of data patterns including PRBS/PRWS. These modules, plus at least one **clock module,** which generates the common system frequency of the instrument, are installed in the mainframe.

The VXI frame offers 13 slots. Assuming the use of the FireWire interface and one Clock module in place, the mainframe can hold up to 10 channels at 13.5 Gbit/s, 11 channels at the data rate of 10.8 Gbit/s, 22 channels at 3.35 Gbit/s, 2.7 Gbit/s and 1.65 Gbit/s or 44 channels at 675 Mbit/s. If more channels are needed there is the possibility of adding up to two expander frames to reach the maximum number of channels within one clock group. Additional clock modules are needed to set up systems which work with different clock speeds that are not divisible or multipliable by the factors 2, 4, 8, 16 (if E4832A is used) and 2 and 4 (if E4861A is used). For example, for testing 1:7 or 1:10 Mux/Demux devices two clock modules are required. Please check the Application Examples within the next chapter.

The ParBERT **81250 Software Suite** runs on an external PC, or a laptop, which is connected to the system via an IEEE 1394 PC link to VXI. The operating system is MS Windows® NT 4.0 or Win 2000. The ParBERT 81250 Software Suite consists of:
- Graphical User Interface
- Measurement Suite
- Software Tools (10GbE Tool, SONET/SDH Frame Generator
- VXI Plug & Play Driver

At runtime the software consists of several processes, see new figure. The firmware server controls the hardware and is the link between the graphical user interface and the Hardware Modules. Also the Measurement Software or any custom remote program can communicate with the Firmware Server. The remote access is established either by using the Plug and Play drivers from Agilent Vee or from a C/C++/Visual Basic program or by a SCPI based language via GPIB. This allows the building of a customized VXI system including other standard VXI modules.

**Table 6 gives an overview on key specifications of the different speed classes:**

| | 675 Mbit/s | 2.7 Gbit/s/3.35 Gbit/s | 10.8 Gbit/s | 13.5 Gbit/s |
|---|---|---|---|---|
| Data Rate Range | 333.3 Kbit/s .. 675 Mbit/s | 333.4 Mbit/s .. 2.7 Gbit/s<br>20.8 Mbit/s .. 3.35 Gbit/s | 9.5 .. 10.8 Gbit/s | 500 Mbit/s .. 13.5 Gbit/s |
| Number of Channels within 1 Frame / + 2 Expander Frames with ext. PC | 44/132 | 22/66 | 11/33 | 10/30 |
| Inputs/Outputs | differential & single ended | differential & single ended | differential & single ended | differential & single ended |
| Data Capability | PRBS/PRWS/ 2 Meg Memory | PRBS/PRWS/ 8/16 Meg Memory | PRBS/PRWS/ 32 Meg Memory*** | PRBS/PRWS/ 64 Mbit Memory |
| Generator Formats | DNRZ, RZ, R1 | 2.7G:DNRZ 50% clock<br>DNRZ, R1, RZ | DNRZ, separate clock output** | NRZ, DNRZ |
| Technology addressed | TTL, (P)ECL, LVDS | CML, (P)ECL*, LVDS, SSTL-2 | CML, ECL,LVDS, SSTL-2 | LVDS, CML, PECL, ECL, low voltage CMOS |

**Notes: * for PECL a BIAS Tee at Analyzer input is needed**
**** separate clock output is single ended only**
***** balanced pattern only**

**Table 6: Key Specifications of ParBERT channels**

# E4861A ParBERT 2.7 Gb/s / 1.65 Gb/s Data Module
# E4862A ParBERT 2.7 Gb/s Generator Front-End
# E4863A ParBERT 2.7 Gb/s Analyzer Front-End
# E4864A ParBERT 1.65 Gb/s Generator Front-End
# E4865A ParBERT 1.65 Gb/s Analyzer Front-End
Technical Specifications

## E4861A Generator/Analyzer Module

This module holds any combination of up to two analyzer front-ends (E4863A, E4865A) and generator front-ends (E4862A, E4864A).

With front-ends E4864A and E4865A the maxiumum speed is limited to 1.65 Gbit/s. The maximum speed of 2.7 Gbit/s is achieved with front-ends E4862A and E4863A.

## Clock Module/Data Mode

The generator can operate in clock mode or data mode. Clock mode is achieved when the generator is assigned as a Pulse Port. Data mode is achieved when using it as a Data Port. In clock mode there is a fixed duty cycle of 50%. In data mode there is NRZ format with variable delay. The analyzer always works as Data Port with variable sampling delay. The sampling delay consists of two elements: the start delay and the fine delay. The fine delay can be varied within ±1 period without stopping.

### Data Capabilities

PRBS/PRWS and memory-based data are defined by segments. Segments are assigned to a generator for a stimulating pattern, on an analyzer it defines the expected pattern which the incoming data are compared to. The expected pattern can be set up with mask bits.

The segment length resolution is the resolution to which the length of a pattern segment or mask can be set. The maximum memory per channel of the E4861A can be set in steps of 64 bits up to a length of 8192 kbits. If the 64 bit segment length resolution is too coarse, memory depth and frequency can be traded.

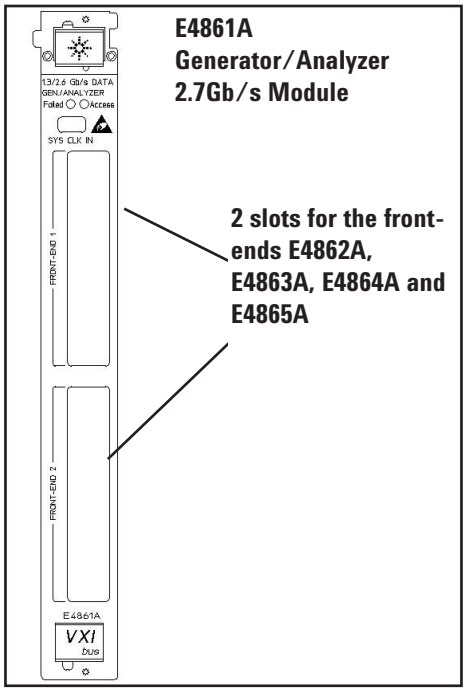



**Figure 1: E4861A Module**

| **Table 1: E4861A Data Generator Timing Specifications (@ 50 % of amplitude, 50 Ohm to GND)** | |
|---|---|
| **Frequency range*** Clock/Data mode 333.334 Mbit/s to 2.70 Gbit/s (1.65Gbit/s E4864A, E4865A) | |
| **Delay (between channels)** | Can be specified as leading edge delay in fraction of bits in each channel |
| **Range** | 0 to 300 ns (not limited by period) |
| **Resolution** | 1 ps |
| **Accuracy** | ±50 ps ±50 ppm relative to the zero-delay placement. (From 20°C to 35°C without autocol)<br>±80 ps ±50 ppm typ. relative to the zero-delay placement and temperature change within ±5°C after autocalibration |
| **Skew between modules of same type** | 50 ps typ. after deskewing at customer levels and unchanged system frequency |
| **Pulse width** | 50% of period typ. in clock mode |

***See tables for front-end deratings**

| **Table 2: E4861A Analyzer Timing All timing parameters are measured at ECL and levels, terminated with 50 Ohm to GND** | |
|---|---|
| **Sample delay= start delay + fine delay,** fine delay can be changed without stopping | |
| **Sampling rate*** | Same as generator |
| **Fine delay range** | ±1 period |
| **Sampling delay range** | Same as generator |
| **Accuracy** | Same as generator |
| **Resolution** | Same as generator |
| **Skew** | Same as generator |

***See tables for front-end deratings**

| Table 3: E4861A Pattern and Sequencing | |
|---|---|
| **Patterns:** | |
| **Memory-based** | up to 8Mbit |
| **PRBS/PRWS** | $2^n$-1, n=7, 9, 10, 11, 15, 23, 31 |
| **Marker Density** | 1/8, 1/4, 1/2, 3/4, 7/8 at PRBS/PRWS $2^n$-1, n=7, 9, 10, 11,15 |
| **Errored** | $2^n$-1, n=7, 9, 10, 11, 15 |
| **Extended ones or zeros** | $2^n$-1, n=7, 9, 10, 11, 15 |
| **Clock patterns** | Divide or multiplied by 2, 4, 8, 16 |
| **User** | Data editor, file import |
| **Analyzer Auto-** | On PRBS or memory-based data |
| **Synchronization:** | manual or automatic by:<br>Bit synchronization* with or without automatic phase alignment<br>Automatic delay alignment around start sample delay (Range: ±10ns)<br>BER Threshold: $10^4$ to $10^9$ |

***Bit synchronization on data is achieved by detecting a 48 Bit unique word at the beginning of the segment. Don't cares within the detect word are possible. In this mode no memory-based data can be sent within the same system. If several inputs synchronize the delay difference between the terminals, it must be smaller ±5 segment length resolution.**

**Table 4: Data rate range, segment length resolution, available memory for synchronization and fine delay operation**

| Data rate range M/bits | Segment length resolution | Maximum memory depth, bits |
|---|---|---|
| 333.334...666.666 | 16 bits | 2,097,152 |
| 666.667...1,333.333 | 32 bits | 4,194,304 |
| 1,333.334...2,666.667 | 64 bits | 8,388,608 |

**In general it is possible to set higher values for the segment length resolution and also at lower frequencies than are indicated in the table**

**Table 5: Depending on the capability of generating PRWS and port width, almost all the combinations are possible except the following:**

| PRWS | Port Width |
|---|---|
| $2^7$-1 | No restriction |
| $2^9$-1 | 7 |
| $2^{10}$-1 | 3, 11, 31, 33 |
| $2^{11}$-1 | 23 |
| $2^{15}$-1 | 7, 31 |
| $2^{23}$-1 | 47 |
| $2^{31}$-1 | No restriction |

## Sub-frequencies

For applications requiring different frequencies at a fraction of the system clock, the rate can be divided or multiplied by 1, 2 or 4. This influences the dependency between segment length resolution and maximum memory depth.

## Synchronization

Synchronization is the method of automatically adjusting the proper bit phase for data comparison on the incoming bit stream. The sychronisation can be performed on PRBS/PRWS and memory based data but it is not possible on a mix of PRxs and memory-based data.

There are two types of synchronization
- bit synchronization
- auto delay aligment

Bit synchronization is possible to cover a bit aligment for a totally unknown number of cycles. Using memory-based data, the first 48 bit within the expected data segment will work as Detect Word which the incoming data are compared to. When the incoming data match with the Detect Word, further analysis begins.

Auto Delay aligment is performed by using the analyzer sampling delay. So there is a limited range while this is possible of ±10ns.

Using Auto Delay alignment will provide synchronization with an absolute timing relation between a group of analyzer channels. So skew measurements are possible.

| Table 6: Parameters for Analyzer Front-Ends E4863A 2.7 Gbit/s (E4865A 1.65 Gbit/s) | |
|---|---|
| **Number of channels** | 1, differential or single ended |
| **Impedance** | 50 Ohm typ.<br>100 Ohm differential if termination voltage is switched off |
| **Internal termination voltage (can be switched off)** | -2.0 to +3.0 V |
| **Threshold voltage range** | -2.0 to + 3.0 V |
| **Threshold resolution** | 2 mV |
| **Threshold accuracy** | ± 1% ±20 mV |
| **Input sensitivity (single-ended and differential)** | 50mV typ |
| **Minimum detectable pulse width** | 180 ps typ. at ECL levels |
| **Maximum input voltage range** | Three ranges selectable:<br>-2V to + 1V<br>-1V to +2V<br>0V to 3V |
| **Maximum differential voltage** | 1.8V operating<br>max. 3V |
| **Phase Margin, with ideal input signal**<br>**with generator E4862A** | >1UI - 50 ps<br>> 1UI-75 ps |
| **Auxiliary out** | Swing: 400 mV pp typ., AC coupled |

| Table 7: Parameters for Generator Front-ends E4862A 2.7 Gbit/s (E4864A 1.65 Gbit/s) | |
|---|---|
| **Outputs** | 1, differential or single-ended |
| **Impedance** | 50 Ohm Typ. |
| **Formats** | Clock: Duty cycle 50%±10% typ.<br>Data: NRZ, DNRZ |
| **Output voltage window** | -2.00 to + 3.00 V<br>3.00 V to 4.5(terminated to +3V only) |
| **Maximum external voltage** | - 2.2 to +4.7 V |
| **External termination voltage** | -2V to +3V |
| **Amplitude/Resolution** | low voltage CMOS 0.05 to 1.8 Vpp*/10 mV |
| **Accuracy HiLevel/Amplitude** | ±2% ±10 mV |
| **Short circuit current** | 72 mA max. |
| **Transition times (20%-80%)** | 90ps typ @ ECL,LVDS<br>110ps typ @ Vpp max |
| **Overshooting/ringing** | 20% + 20mV typ |
| **Jitter, Data mode** | <50ps peak-to-peak |
| **Clock mode** | <5ps, rms |

***does double into open, but outputs may switch off**

# Input/Output

## Addressable technologies

**LVDS, ECL (terminated with 50 to 0 V/-2 V), PECL (terminated to +3 V Analyzer input requires use of a Bias Tee).**

## Analyzer Input

The analyzer channel can be operated:

- Single-ended normal
- Single-ended compliment
- Differential

For termination there is always 50 Ohm connected to a programmable termination voltage. In differential mode there is an additional, selectable 100 Ohm differential termination. Independent of the selected termination, there is the choice of whether the anaylsis of the incoming signal is performed on the input or true differentially. For connecting to PECL it is recommended a Bias Tee is used. The 2.7 Gb/s analyzer offers an auxiliary output, where the differential input signal is available as a single-ended signal. The bandwidth of the Aux Output is limited to 2GHz.

## Generator Output

The Generator output can be used as single-ended or differential. Enable/Disable relays provide on/off switching. When switched off internal termination is provided. It is recommended that unused outputs are either turned off or externally terminated.

The Generator outputs can work into 50 Ohm centre tapped termination or 100 Ohm differential termination. The proper termination scheme can be chosen from the editor to adapt proper level programming.

## Protection

Input and Output Relays switch off automatically if maximum voltages are about to be exceeded.

# E4809A 13.5 GHz Central Clock Module
# E4808A High Performance Central Clock Module
# E4805B 675 MHz Central Clock Module
Technical Specifications

Each ParBERT 81250 system consists of at least one clock module, which generates the system clock for at least one generator or analyzer or any mix.
Please see the table to the right for a complete compatibility overview!

| Modules/Central Clock | E4805B | E4808A | E4809A |
|---|---|---|---|
| E4832A - ParBERT 675 Mb/s | • | • | • |
| E4861A - ParBERT 2.7/1.6 Gb/s | • | • | |
| E4861B - ParBERT 3.35 Gb/s | | • | • |
| E4810A/11A - ParBERT 3.3.5 Gb/s optical | | • | • |
| E4866A/67A - ParBERT 10.8 Gb/s | | • | |
| N4872A/73A - ParBERT 13.5 Gb/s | | | • |
| E4868B/69B - ParBERT 45 Gb/s | | • | |

**Sequencing**
The sequencing can be used to specify the data flow:
- single
- looped
- infinitely
- event handling (branch)
- synchronization.

**Event Handling**
With the event handling the flow of data generation and Analysis can be influenced with external signals at run time.
**Usage of Events:**
- stop and go of data
- match loop
- intergration with other equipment (ATE)
- trigger on error

**Master slave, multi-mainframe, different clock groups.**
Up to 3 clock modules can be combined to run in one clock grouping by connecting the master slave cable. This is used to combine channels which do not fit into one frame into one clock group. Omitting the master-slave connection will run the channels within separated clock groups. A system can be operated using different clock groups. So a bunch of channels are combined with a clock module. The frequencies used can be totally asynchronous or m/n ratio (see clock input multiplier/divider). For separated clock groups the master slave must not be connected. Within one system the modules must always be of the same type.

| E4809A, E4808A and E4805B Sequencing Features | |
|---|---|
| **Number of Segments** | 1 to 30 (every segment looped once)<br>1 to 60 (no segment looped) |
| **Looping levels** | Up to 4 nested loops plus one optional infinite loop<br>Loops can be set independently from 1 to 2 repetitions |
| **Start/stop** | External input, manual, programmed (stop with E4832A only) |
| **Event handling** | React on internal and external events. Details see next table |

| E4809A, E4808A and E4805B Event Handling |
|---|
| **Event trigger sources** |
| Events can be defined as any combination of the following sources.<br>A maximum of 10 events can be defined. |
| - 8-line trigger input pod for TTL signals |
| - VXI trigger lines TO and T1 |
| - Any capture error/or no error detected by one of the analyzer channels |
| - Software command control: an event trigger command issued locally or remotely |
| **Reactions to an event** can be set per data segment immediately or deferred and can be any combination of: |
| - Data segment jump |
| - Launch trigger pulse to the trigger output of the Clock Module |
| - VXI trigger lines TO and T1 can be set to 01, 10 or 11 |

| E4809A, E4808A and E4805B Trigger Pod characteristics | | |
|---|---|---|
| **Input Lines** | 8, single-ended | |
| **Input levels** | TTL compatible | |
| **Input threshold** | 1.5 V | |
| **Input termination** | 5 k Ohm pullup to +5 V | |
| **Absolute max. ratings for input voltages** | -1.2 V to + 7.0 V | |
| **Cable delay** | 11 ns typical | |
| **sampling clock frequency** | system frequency/segment length resolution | |
| | TRIGGER OUTPUT | CLOCK/REF INPUT |
| **Setup time*** | 2.5ns | -12.5ns |
| **Hold time *** | 5 ns | 20 ns |

***includes the cable delay**

## Clock Input

This input runs ParBERT synchronously with an external clock. Usage of a continuous clock is necessary. Burst clock can not be used as an external clock. Two modes are selectable: Indirect external clock mode (clock module PLL is used) and Direct external clock mode (clock module is bypassed).

| Clock Input | |
|---|---|
| **Clock Input** | AC coupled; 3.5mm(f) |
| **Frequency range** | |
| **Indirect mode** | 20.834MHz...13.5GHz |
| **Direct mode** | 500MHz...13.5GHz |
| **Clock Input (Indirect mode only)** | m=1...256; n=1...256 |
| **Multiplier(m)/divider(n)** | m*n<=1024; m/n*input frequency must fit data range input frequency/n>=1,3MHz |
| **Input transition/slope** | 30 ps typ. |
| **Zin** | 50 Ohm |
| **Sensitivity** | <150mV |

## Trigger Output

This output will be used to deliver a trigger signal to a DUT, a Digital Communication Analyzer (Agilent 86100B Series) or as a stimulus for the Analyzer deskew.

| Trigger Output | |
|---|---|
| **Trigger Output** | DC coupled, SMP (f) |
| **Frequency** | Tbd |
| **Output transition/slope** | 70 ps typ. 10/90 |
| **Zout/Termination voltage** | 50 Ohm / -2 to +3V |
| **Output voltage window** | -2V to +3V |
| **Output level** | 0.1 to 1.8 Vpp |

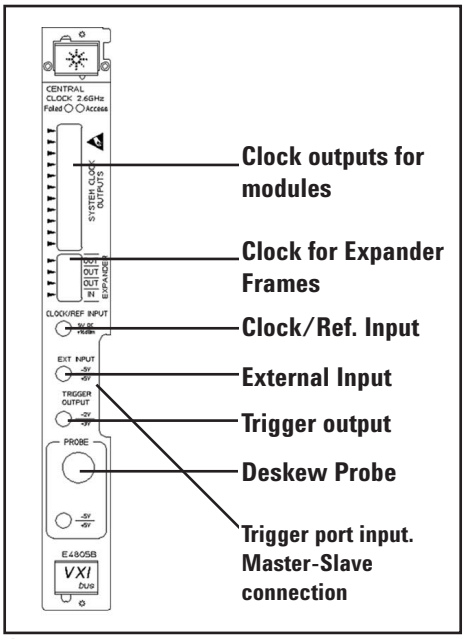
## E4805B and E4808A Central Clock Modules

The central clock module includes a PLL (Phase-Locked Loop) frequency generator to provide a system clock. Depending on the frequency chosen, the data modules can be clocked at a ratio of 1, 2, 4, 8, 16, 32, 64 or 256 times higher or lower than the system clock.

**External start/stop:** The data running can be started by an external signal applied to the external input. With module E4832A there is also Stop and Gate mode.

**Ext. Clock/Ext. Reference:** This input runs ParBERT 81250 synchronously with an ext. clock, or when a more accurate reference is needed than the internal oscillator. Usage of a continuous clock is necessary. Burst clock cannot be used as an external clock. Maximum external clock is 2.7 GHz for the E4805B and 10.8Gbit/s for the E4808A. (Note: no improvement of jitter specifications will be achieved).

**Guided deskew:** Individual semi-automatic deskew per channel. The deskew probe 15447A allows deskew on the DUT's (Device Under Test) fixture.




**Clock Module**

**E4805B and E4808A Clock Module specifications**

| | E4805B | E4808A |
|---|---|---|
| **Frequency range*** | 1kHZ to 675 MHZ | 170 kHz to 675 MHz |
| **(can be entered as period or frequency)** | E4805B will run with: | E4808A will run with: - E4866A/E4867A in range of 9.5GHz to 10.8GHz |
| **E4808A Clock Module specifications** | - E4861A in range of 334 MHz to 2.7GHz - E4832A in range of 334KHZ to 675 MHz | - E4861B in range of 20.834 MHz to 3.35GHz- E4861A in range of 334 MHz to 2.7GHz - E4832A in range of 334KHZ to 675 MHz |
| **Resolution** | 1 Hz | 1 Hz |
| **Accuracy** | ±50 ppm with internal PLL reference | ±50 ppm with internal PLL reference |

**May be limited or enhanced by modules or frontends**

| External input and ext. clock/ext. ref. input | E4805B | | E4808A | |
|---|---|---|---|---|
| **Zin/Termination voltage** | 50 Ohm/-2.10 V to 3.30 V | | 50 Ohm /-2.10 V to 3.30 V | |
| **Sensitivity/max levels** | 400 mVpp /-3 V to + 6 V | | 200 mVpp /-3 V to + 6V for < 9.5Gbit/s<br>300mVpp/-3V to+ 6V for > 9.5 Gbit/s | |
| **Coupling**<br>**Ext. Input:** | dc,<br>Threshold Range: -1.40 V to +3.70 V | | dc,<br>-1.40 V to +3.70 V | |
| **Ext. Clock/Ext. Ref:** | ac | | ac | |
| **Input transitions/slope** | < 20ns. Ext. input active edge is selectable | | < 20 ns. Ext. Input active edge is selectable | |
| **Clock input multiplier(m)/ divider (n)** | m=1...256; n=1...256<br>m*n<=1024 m/n * input frequency must fit data range input frequency/n>=1.3 MHZ | | | |
| **PLL lock time** | 100ms | | 100 ms | |
| **Input frequency/period**<br>**Ext. Clock** | 170 kHz - 2.7 GHz | | 170 kHz - 10.8 GHz | |
| **Ext. Ref** | 1*, 2*, 5, or 10 MHz | | 1*, 2*, 5, or 10 MHz | |
| **Required duty cycle** | 50 ±10 % | | 50 ±10 % | |
| **Latency (typical):** | to trigger Output | to channel output | to trigger Output | to channel Output |
| **Ext. input** | 16ns ±1 clock | 46ns ±1 clock | 16ns ±1 clock | 46ns ±1 clock** |
| **Ext. clock** | 15ns | 45ns | 15ns | 45ns |
| | Add 3ns if an expander frame is used | | Add 3 ns if an expander frame is used | |

*** Jitter performance may be degraded**

**** If frequency=667MHz**

**Trigger Ouput**

Can be used in:

- clock mode
- sequence mode

In sequence mode a pulse will be set to mark the start of any segment

The trigger output runs to a maximum 675MHZ. If a higher speed performance clock is needed;

- A 2.7GHZ Clock can be obtained from a 2.7Gb/s channel operated as a pulse port.
- A 10.8GHZ clock is available from the 10.8 Gb/s generated module as clock output.

| Trigger output characteristics E4805B and E4808A | |
|---|---|
| **Trigger output signals** | - Clock mode (up to 675 MHz).<br>- Sequence Mode |
| **Output impedance** | 50 Ohm typ. |
| **Output level** | TTL (frequency < 180 MHz), 50 Ohm to GND<br>ECL 50 Ohm to GND/-2 V, PECL 50 Ohm +3V |
| **Trigger advance** | 30 ns typ. between trigger output and data output/sampling point (delay set to zero in both cases) |
| **Maximum ext voltage** | -2 V to +3.3 V |
| **Jitter (int. reference/int. clock)** | < 10 ps rms (5ps typ. ) |

# General Characteristics

**Mainframes:** See table 34.

**Save/recall:** Pattern segments, settings and complete settings plus segments can be saved and recalled. The number of settings that can be stored is limited only by internal disk space.

**Vector import/export:** Pattern files can be imported/exported via a 3.5 inch floppy disk, LAN or GP-IB (IEEE 488.2). File format is ASCII using a STIL subset.

**Programming interface:** GP-IB (IEEE 488.2) and LAN. The interface to applications such as C, Visual Basic, or VEE must be installed. Agilent 81200 Plug & Play drivers for easy programming are available.

**Programming language:** SCPI 1992.0

**Programming times:** Vector transfer from memory to hardware depends on the amount of data.

**On-line help:** Context-sensitive.

**Print-on-demand:** Getting started and programming guides can be printed from .pdf files included in the ParBERT 81250 software.

**Self-test:** Module and system self-tests can be initiated.

## Modules

**Module size:** VXI C-size, 1 slot.

**Module type:** Register-based; requires ParBERT 81250 user software E4875A supplied with the mainframes.

**Weight:** (including front-ends) Net: 2kg.

**Shipping:** 2.5 kg.

**Warranty:** 3 years return for repair service, depending on support option.

**Re-calibration period:** 1 year.

**Agilent Technologies Quality Standards**
The ParBERT 81250 is produced to the ISO 9001 international quality system standard as part of Agilent Technologies' commitment to continually increasing customer satisfaction through improved quality control.

**Table 41: Programming Times**

| | **Programming time** |
|---|---|
| **Change of levels** | 6 ms typ. |
| **Change of delay** | 16 ms. typ. Not applicable in run mode. |
| **Change of period** | 60 ms typ. For one E4805B with one E4832A. Not applicable in run mode. Increases with the number of modules but less than proportional. |
| **Stop + start** | 32 ms typ. |
| **Synchronization*** | 50ms typ. (without phase alignment)<br>110ms typ. with 20% phase accuracy @ 660MHz<br>650ms typ. with 1% phase accuracy @ 660MHz |
| **Download values**: | |
| System with 4 channels, 100,000 bit each | < 1.5 s typ. |
| System with 120 channels, 1 Mbit each | < 30 s typ. |
| System with 40 channels, 1 Mbit each | < 10 s typ. |

*Add numbers for each synchronizing analyzer within one module

**Table 42: Power Requirements of Modules and Front-Ends**

| | DC Volts | +24V | +12V | +5V | -2V | -5.2V | -12V |
|---|---|---|---|---|---|---|---|
| **Modules (These specifications are valid for the module with the front-ends installed)** | | | | | | | |
| E4805B Central Clock module | DC Current | 0.15A | 0.2A | 1.8A | 1.4A | 3.8A | 0.2A |
| | Dynamic current | 0.0015A | 0.02A | 0.18A | 0.14A | 0.38A | 0.02A |
| E4808A | DC Current | .35A | 0.2A. | 3.0A | 1.2A | 3.6A | 0.2A |
| | Dynamic current | 0.04 A | 0.02A | 0.30 A | 0.12A | 0.36A | 0.02A |
| E4867A | DC Current | 0.2A | 1.0A | 7.0A | 1.5A | 3.0A | 0.8A |
| | Dynamic current | 0.02A | 0.1A | 0.7A | 0.15A | 0.3A | 0.08A |
| E4866A | DC Current | 0.2A | 1.0A | 5.0A | 1.2A | 2.6A | 0.5A |
| | Dynamic Current | 0.02A | 0.1A | 0.5A | 0.12A | 0.26A | 0.05A |
| E4861A 2.7 Gbit/s Gen./An.Module | DC Current | 0.10 | 0.50A | 5.20A | 1.80A | 4.00A | 0.90A |
| | Dynamic current | 0.01A | 0.05A | 0.52A | 0.18A | 0.40A | 0.09A |
| Remark: The power requirements of E4861A include the power requirements of any two front ends | | | | | | | |
| E4861B | DC Current | 0.02A | 0.02A | 1,8A | 0,33A | 0,04A | 0,A |
| | Dynamic current | 0,01A | 0,01A | 0,2A | 0,03A | 0,05A | 0,A |
| E4832A 675 Mbit/s Gen./An. Module | DC Current | 0.10A | 0.10A | 2.60A | 0.60A | 3.60A | 0.10A |
| | Dynamic Current | 0.01A | 0.001A | 0.26A | 0.06A | 0.36A | 0.01A |
| Remark: For the module E4832A, the power specifications of the chosen front-ends (E4835A, E4838A or E4843A) have to be added to the power specifications of the E4832A module to get the overall value of the power specifications | | | | | | | |
| **Front-ends** | | | | | | | |
| E4835A two differential Analyzer 675 Mbit/s (E4835AZ) | DC Current | | 0.2A | 1.2A | 0.2A | 0.3 A | 0.3A |
| | Dynamic Current | | 0.02A | 0.12A | 0.02A | 0.03A | 0.03A |
| E4838A Differential Generator 675 Mbit/s MHz,var. Slopes | DC Current | | 0.45A | 0.18A | 0.07A | 0.38A | 0.41A |
| | Dynamic Current | | 0.045A | 0.006A | 0.007A | 0.038A | 0.041A |
| E4862B Generator | DC Current | 0,2A | 0,2A | 0,7A | 0,2A | 0,5A | 0,21A |
| | Dynamic Current | 0.02A | 0,02A | 0,07A | 0,02A | 0,05A | 0,02A |
| E4863B Analyzer | DC Current | 0,2A | 0,2A | 1,8A | 0,2A | 0,5A | 0,21A |
| | Dynamic Current | 0,02A | 0,02A | 0,2A | 0,02A | 0,05A | 0,02A |

**Table 43: Cooling requirements for modules with front-ends installed**

| Modules | $\Delta P$ mm $H_2O$ 10°C rise | Air Flow Liter/s |
|---|---|---|
| E4805B | 0.25 | 3.6 |
| E4808A | 0.25 | 3.6 |
| E4832A | 0.30 | 4.7 |
| E4861A | 0.40 | 5.2 |
| E4861B* | 0.40* | 6.6 |
| E4866A | 0.30 | 5.2 |
| E4867A | 0.30* | 5.5 |

* 15°C rise

| | |
|---|---|
| **Operating temperature** | 10 °C to 40 °C |
| **Storage temperature** | -20°C to +60°C |
| **Humidity** | 80% rel. humidity at 40 °C |
| **Power requirements** | 90-264 Vac, ± 10%, 47-66 Hz ,<br>90-264 Vac, ± 10%, 300-440 Hz (not recommended<br>leakage current may exceed safety limits @ > 132 Vac) |
| **Power available for modules** | 950 W for 90-110 Vac supplies<br>1000 W for 110-264 Vac supplies |
| **Electromagnetic compatibility** | EN 55011/CISPR 11 group 1, class A + 26 dB |
| **Acoustic noise** | 48 (56) dBA sound pressure at low (high) fan speed |
| **Safety** | IEC 348, UL1244, CSA 22.2 #231, CE-mark |
| **Physical dimensions** | W: 424.5 mm, 16.71 inches<br>H: 352 mm, 13.85 inches<br>D: 631 mm, 24.84 inches |
| **Weight (Net)** | 26.8 kg 25.3 kg |
| **Weight (shipping)(max.)** | 72 kg 67 kg |