The HP 1660E and 1670E-Series Benchtop Logic Analyzers

Technical Data

Affordable logic analyzers designed for your exact needs

HP's new family of benchtop logic analyzers includes four new series of products, enabling design engineers to purchase an affordable logic analyzer that meets their exact needs and matches their budget. The units include a VGA resolution color flat panel display to help you find information quickly and the well designed user interface gets you to the answer in less time. Users can use either a mouse or the front panel to easily navigate through the user interface. An optional PC style keyboard is also supported. A compact all-in-one design also helps save space on a crowded lab bench.

The HP 1660ES-Series models come with a built-in, 500-MHz, 2-GSa/s oscilloscope that can be triggered by the logic analyzer. Some of the tougher hardware debug problems can be found only with the digital triggering capabilities of a logic analyzer and can only be solved with the analog resolution of an oscilloscope.

The pattern generator capability in the HP 1660EP-Series allows designers to substitute for missing sub-systems during development.

The HP 1670E-Series help simplify the capture and analysis of complex events with 1M deep memory. Deep memory is a valuable logic analyzer feature for debugging embedded microprocessor systems.

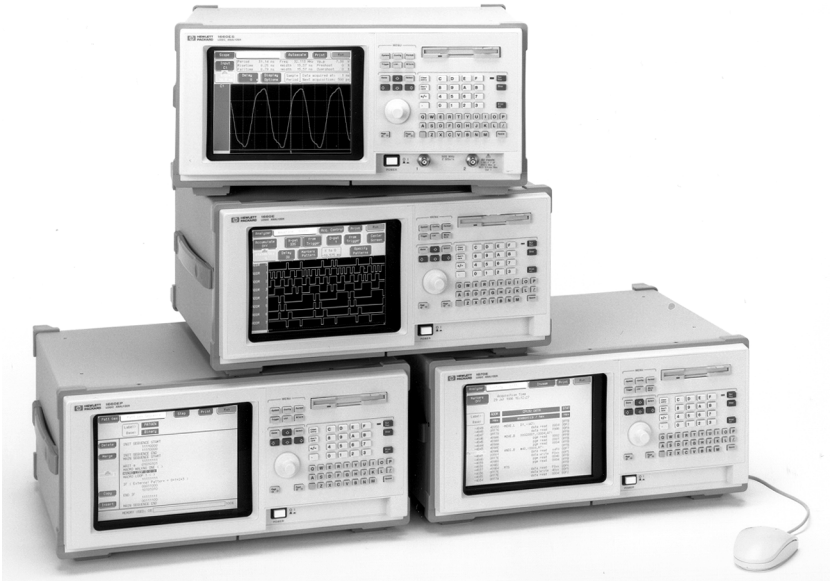


Figure 1. HP's new family of benchtop logic analyzers with color displays

Model Number	HP 1660E	HP 1661E	HP 1662E	HP 1663E
Channels	136	102	68	34
Application	General purpose logic analysis			
Model Number	**HP 1660EP**	**HP 1661EP**	**HP 1662EP**	**HP 1663EP**
Channels	136	102	68	34
Application	Hardware simulation and stimulus-response testing with integrated 32-channel pattern generator			
Model Number	**HP 1660ES**	**HP 1661ES**	**HP 1662ES**	**HP 1663ES**
Channels	136	102	68	34
Application	Parametric and mixed-signal testing with integrated two-channel oscilloscope			
Model Number	**HP 1670E**	**HP 1671E**	**HP 1672E**	
Channels	136	102	68	
Application	Complex debugging and troubleshooting with deep memory			

HP 1660E/ES/EP Series Logic Analyzer key Specifications and Characteristics

HP Model Number	1660E/ES/EP	1661E/ES/EP	1662E/ES/EP	1663E/ES/EP	1664A
State and Timing Channels	136	102	68	34	34
Timing Analysis	Conventional: 250 MHz all channels, 500 MHz half channels Transitional: 125 MHz all channels, 250 MHz half channels Glitch: 125 MHz half channels				
State analysis speed	100 MHz, all channels				50 MHz
State Clock/Qualifiers	6	6	4	2	2
Memory Depth per Channel	4k per channel, 8k in half-channel modes				
LAN Port	Standard for all E/ES/EP models				N/A

HP 1660EP Series Pattern Generator Key Specifications and Characteristics

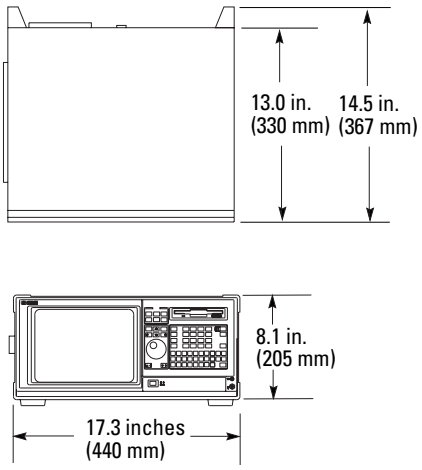
HP Model Number	1660EP, 1661EP, 1662EP, 1663EP		
Maximum Clock Speed	200 MHz	100MHz	50 MHz
Number of Data Channels	16	32	32
Memory Depth, in vectors	258,048	258,048	258,048
"IF" Command	No	No	Yes

HP 1670E-Series Logic Analyzer Key Specifications and Characteristics

HP Model Number	1670E	1671E	1672E
State and Timing Channels	136	102	68
Timing Analysis	Conventional: 125 MHz all channels, 250 MHz half channels		
State Analysis Speed	100 MHz, all channels		
State Clocks/ Qualifiers	4	4	4
Memory Depth per Channel	1M per channel, 2M in timing half-channel mode		

HP 1660ES Series Oscilloscope Key Specifications and Characteristics

HP Model Number	1660ES, 1661ES 1662ES, 1663ES
Channels	2
Maximum Sample Rate	2 GSa/s per channel
Bandwidth	dc to 500 MHz (dc coupled)
Rise Time	700 ps
Vertical Resolution	8 bits
Memory Depth per Channel	32k samples



Weight = 28.6 lbs. (13kg)

Figure 3. Logic analyzer dimensions and weight

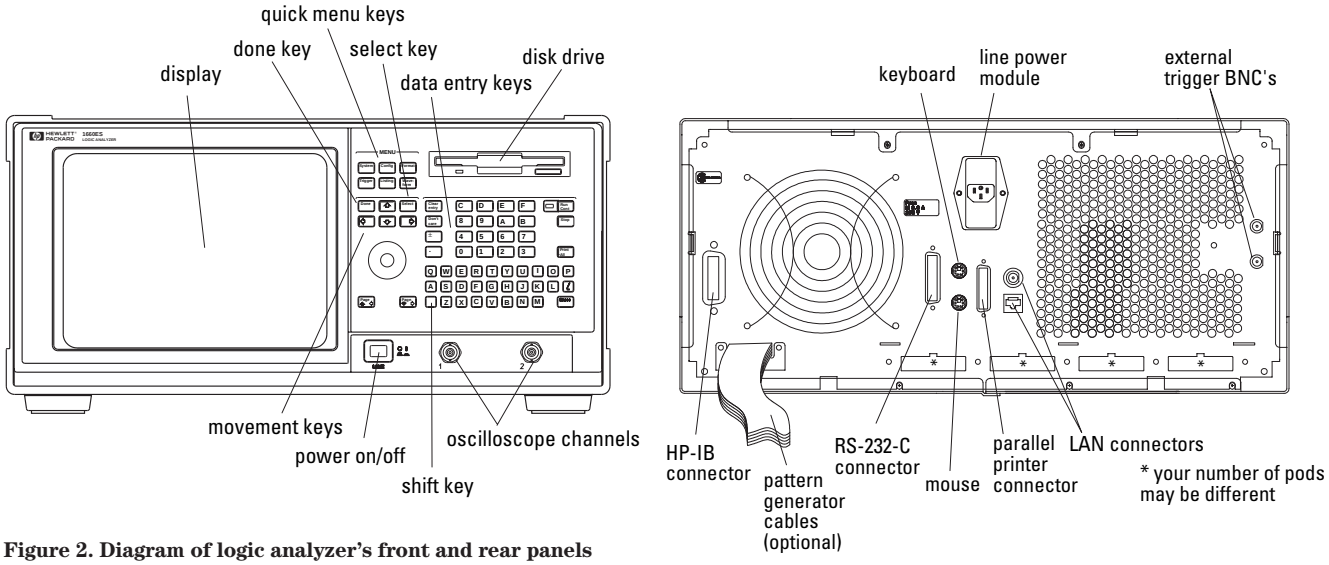


Figure 2. Diagram of logic analyzer's front and rear panels

HP 1660E and 1670E-Series Logic Analyzer Specifications and Characteristics

Human Interface

Front Panel	A knob and keypad make up the front-panel human interface. Keys include control, menu, display navigation, and alpha-numeric entry functions.
Mouse	A DIN mouse is shipped as standard equipment. It provides full instrument control. Knob functionality is replicated by holding down the right button and moving the mouse left or right. [1]
Keyboard	The logic analyzer can also be operated using a DIN keyboard. Order the HP Logic Analyzer Keyboard Kit, model number HP E2427B. [1]

Input/Output, Control, and Printing

I/O Ports	All units ship with a Centronics parallel printer port, RS-232, and HP-IB as standard equipment.
LAN Interface	An Ethernet LAN interface is standard. The LAN interface comes with both Ethertwist and ThinLan connectors. The LAN supports FTP and PC/NFS connection protocols. It also works with X11 windows packages. [1]
Programmability	Each instrument is fully programmable from a computer via HP-IB, RS-232 and LAN connections. [1]
HP Printer Support	Printers which use the HP Printer Control Language (PCL) and have a parallel Centronics, RS-232 or HP-IB interface are supported: HP DeskJet, LaserJet, QuietJet, PaintJet, and ThinkJet models
Alternate Printers Supported	The Epson FX80, LX80 and MX80 printers with an RS-232 or Centronics interface are supported in the Epson 8-bit graphics mode.
Hard Copy Output	Screen images can be printed in black and white or color from all menus using the *Print* field. State or timing listings can be also be printed in full or part (starting from center screen) using the *Print All* selection.

Mass Storage Files and Software

Updating the Operating System	The operating system resides in Flash ROM and can be updated from the flexible disk drive or from the internal hard disk drive. [1]
Mass Storage	Supported by an internal hard disk drive and by a 1.44 Mbyte, 3.5-inch flexible disk drive. Supports DOS and LIF formats. [1]
Screen Image Files	An image file of any display screen can be stored to disk via the display's *Print* field in black & white or color TIFF, color PCX, or black & white Encapsulated PostScript™ (EPS) formats.
ASCII Data Files	State or timing listings can be stored as ASCII files on a disk via the display's *Print* field. These files are equivalent in character width and line length to hard-copy listings printed via the *Print All* selection.
Configuration and Data Files	Logic analyzer and oscilloscope files that include configuration and data information (if present) are encoded in a binary format. They can be stored to or loaded from the hard disk drive or a flexible disk.
Recording of Acquisition and Storage Times	Binary format configuration/data files are stored with the time of acquisition and the time of storage.[1]

Acquisition Arming

Initiation	Arming is started by *Run, Group Run,* or the Port In BNC.
Cross Arming	Analyzer machines and the oscilloscope or pattern generator can cross-arm each other.
Output	An output signal is provided at the Port Out BNC.
PORT IN Signal and Connection	Port In is a standard BNC connection. The input operates at TTL logic signal levels. Rising edges are valid input signals.
PORT OUT Signal and Connection	Port Out is a standard BNC connection with TTL logic signal levels. A rising edge is asserted as a valid output.
Skew Adjustment	Correction factors for nominal skew between displayed timing and oscilloscope signals are built into the operating system. Additional correction for unit-by-unit variation can be made using the *Skew* field. An entered skew value affects the next (not the present) acquisition display.

1] Please refer to HP 1664A Product Specifications and Characteristics on page 7.

HP 1660E and 1670E-Series Logic Analyzer Specifications and Characteristics (cont.)

PORT IN Arms Logic Analyzer [2]	15 ns typical delay from signal input to a *don't care* logic analyzer trigger.
PORT IN Arms Oscilloscope	40 ns typical delay from signal input to an *immediate* oscilloscope trigger.
Logic Analyzer Arms PORT OUT [2]	120 ns typical delay from logic analyzer trigger to signal output.
Oscilloscope Arms PORT OUT	60 ns typical delay from oscilloscope trigger to signal output.

Operating Environment

Power	115 Vac or 230 Vac, –22% to +10%, single phase, 48-66 Hz, 320 VA max
Temperature	Instrument, 0° to 50° C (+32° to 122° F). Disk media, 10° to 40° C (+50° to 104°F). Probes and cables, 0° to 65° C (+32° to 149° F)
Humidity	Instrument, up to 95%, relative humidity at +40° C (+140° F). Disk media and hard drive, 8% to 85% relative humidity.
Altitude	To 3,048 m (10,000 ft) [1]
Vibration: Operating	Random vibrations 5–500 Hz, 10 minute per axis, ~ 0.3 g (rms).
Vibration: Non Operating	Random vibrations 5–500 Hz,10 minutes per axis,~ 2.41 g (rms); and swept sine resonant search, 5–500 Hz, 0.75 g (0-peak), 5 minute resonant dwell @ 4 resonances per axis.

[1] Please refer to HP 1664A Product Specifications and Characteristics on page 7.

[2] Time may vary depending upon the mode of logic analyzer operation.

* Warranted specification.

[3] Full channel /half channel modes

Physical Factors

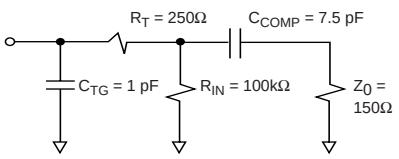
Safety	IEC 348/ HD 401, UL 1244, and CSA Standard C22.2 No. 231 (series M-89)

EMC

CISPR 11:1990/EN 55011 (1991):
Group 1 Class A
IEC 801-2:1991/EN 50082-1 (1992):
4kV CD, 8 kV AD
IEC 801-3:1984/EN 50082-1 (1992): 3 V/m
IEC 801-4:1988/EN 50082-1 (1992): 1kV

Logic Analyzer Probes

Input Resistance	100 kΩ ±2%
Input Capacitance	approx. 8 pF (see figure 4)



High Frequency Model for Probe Inputs

Figure 4

Minimum Input Voltage Swing	500 mV peak-to-peak
Minimum Input Overdrive	250 mV or 30% of input amplitude, whichever is greater
Threshold Range	–6.0 V to +6.0 V in 50-mV increments
Threshold Setting	Threshold levels may be defined for pods (17-channel groups) on an individual basis
Threshold Accuracy*	± (100 mV +3% of threshold setting)
Input Dynamic Range	± 10 V about the threshold
Maximum Input Voltage	± 40 V peak
+5 V Accessory Current	1/3 amp maximum per pod
Channel Assignment	Each group of 34 channels (a pod pair) can be assigned to Machine 1, Machine 2 or remain unassigned. The HP 1663E/ES/EP and the HP 1664A do not have a Machine 2.

State Analysis

Maximum State Speed*	100 MHz[1] all models
Memory Depth per Channel	
HP 1660E/ES/EP Series	4k samples std. Time tags on: 2k samples
HP 1670E Series	1M samples standard Time Tags On: 500k samples Compare Mode On: 250k samples Compare Mode and Time Tags On: 120k samples
State Clocks	Clock edges can be ORed together and operate in single phase, two-phase demultiplexing, or two-phase mixed mode. Clock edge is selectable as positive, negative, or both edges for each clock.
State Clock Qualifier	The high or low voltage level of up to 4 of the 6 clocks can be ANDed or ORed with the clock specification.

Setup/Hold* [4]

one clock, one edge	3.5/0 ns to 0/3.5 ns (in 0.5 ns increments)
one clock, both edges	4.0/0 ns to 0/4.0 ns (in 0.5 ns increments)
multi-clock, multi-edge	4.5/0 ns to 0/4.5 ns (in 0.5 ns increments)

HP 1660E and 1670E-Series Logic Analyzer Specifications and Characteristics (cont.)

Minimum State Clock Pulse Width* [4]	3.5 ns
Minimum Master to Master Clock Time* [4]	10.0 ns
Minimum Slave to Slave Clock Time [4]	10.0 ns
Minimum Master to Slave Clock Time [4]	0.0 ns
Minimum Slave to Master Clock Time [4]	4.0 ns
Clock Qualifiers Setup/Hold [4]	4.0/0 ns (fixed)
State Tagging [5]	Counts the number of qualified states between each stored state. Measurement can be shown relative to the previous state or relative to trigger. Max. count is 4.29×10^9.
Time Tagging [5]	Measures the time between stored states, relative to either the previous state or to the trigger. Max. time between states is 34.4 sec. Min. time between states is 8 ns.
Time Tag Resolution	8 ns or 0.1% (whichever is greater)

Timing Analysis

Conventional Timing	Data stored at selected sample rate across all timing channels.
HP 1660 Series	
Sample Period [3]	4 ns/2 ns minimum, 8.38 ms maximum
HP 1670 Series	
Sample Period [3]	8 ns/4 ns minimum, 41 ms/10 ms maximum
Time Covered by Data [3]	Sample period × memory depth
Transitional Timing	(HP 1660E/ES/EP Series only) Sample is stored in acquisition memory only when the data changes. A time tag stored with each sample allows reconstruction of waveform display. Time covered by a full memory acquisition varies with the number of pattern changes in the data.
Time Covered by Data [3]	16.3 µs minimum, 9.7 hrs./6.5 hrs. maximum
Maximum Time Between Transitions	34.4 s
Number of Captured Transitions [3]	1023-2047/682-4094 Depending on input signals
Glitch Capture Mode	(HP 1660E/ES/EP Series only.) Data sample and glitch information is stored every sample period.
Maximum Timing Speed	125 MHz
Sample Period	8 ns minimum, 8.38 ms maximum
Minimum Glitch Width*	3.5 ns
Maximum Glitch Width	Sample Period – 1 ns
Memory Depth per Channel	2048 samples
Time Covered by Data	Sample Period × 2048: 16.3 µs minimum, 17.1 sec maximum

Time Interval Accuracy

Sample Period Accuracy	± 0.01%
Channel-to-Channel Skew	2 ns typical, 3 ns maximum
Time Interval Accuracy	± (Sample Period Accuracy + channel-to-channel skew + 0.01% of time interval reading)
Maximum Delay After Triggering	Sample Period 2-8 ns : 8.389 ms Sample Period > 8 ns: 1,048,575 × sample period

Trigger Specifications

Trigger Macros	Trigger setups can be selected from a categorized list of trigger macros. Each macro is shown in graphical form and has a written description. Macros can be chained together to create a custom trigger sequence.
Pattern Recognizers	Each recognizer is the AND combination of bit (0,1, or X) patterns in each label. Ten pattern recognizers are available.
Minimum Pattern and Range Recognizer Pulse Width	>125 MHz timing modes: 13 ns + channel-to-channel skew ≤125 MHz timing modes: 1.01 x (1 sample period +1 ns + channel-to-channel skew)

[3] Full Channel /Half Channel Modes

[4] Specified for an input signal VH= – 0.9V, VL = – 1.7V, slew rate = 1V/ns, and threshold = –1.3V

[5] Time or-state-tagging (Count Time or Count State) is available in the full-channel state mode. There is no speed penalty for tag use. Memory is halved when time or state tags are used unless a pod pair (34-channel group) remains unassigned in the Configuration menu.

* Warranted specification.

HP 1660E and 1670E-Series Logic Analyzer Specifications and Characteristics (cont.)

Range Recognizers	Recognize data which is numerically between or on two specified patterns (ANDed combination of zeros and/or ones). Two range recognizers are available.
Range Width	32 channels
Edge/Glitch Recognizers	Trigger on glitch or edge on any channel. Edge can be specified as rising, falling or either.
Edge/Glitch Recognizers	2 (in timing mode only)
Edge/Glitch Recovery Time	Sample Period 2-8 ns: 28 ns Sample Period > 8 ns: 20 ns + sample period
Qualifier	A user-specified term that can be any state, no state, any recognizer, (pattern, ranges or edge/glitch), any timer, or the logical combination (NOT, AND, NAND, OR, NOR, XOR, NXOR) of the recognizers and timers.
Branching	Each sequence level has a branching qualifier. When satisfied, the analyzer will branch to the sequence level specified.
Occurrence Counters	Qualifiers may be specified to occur up to 1,048,575 times before advancing to the next level. Each sequence level has its own counter. The maximum occurrence count is 1,048,575.
Storage Qualification (state only)	Each sequence level has a storage qualifier that specifies the states that are to be stored.

Maximum Sequencer Speed	125 MHz
State Sequence Levels	12
Timing Sequence Levels	10
Timers	Timers may be Started, Paused, or Continued at entry into any sequence level after the first.
Timers	2
Timer Range	400 ns to 500 seconds
Timer Resolution	16 ns or 0.1% whichever is greater
Timer Accuracy	± 32 ns or ± 0.1%, whichever is greater
Timer Recovery Time	70 ns

Acquisition, Measurement and Display Functions

Run	Starts acquisition of data in specified trace mode.
Stop	In single trace mode or the first run of a repetitive acquisition, stop halts acquisition and displays the current acquisition data. For subsequent runs in repetitive mode, stop halts acquisition of data and does not change current display.
Trace Mode	Single mode acquires data once per trace specification; repetitive mode repeats single mode acquisitions until stop is pressed or until pattern time interval or compare stop criteria are met.

Trigger	Displayed as a vertical dashed line in the timing waveform, state waveform and X-Y chart displays and as line 0 in the state listing and state compare displays.
Activity Indicators	Provided in the Configuration, State Format, and Timing Format menus for monitoring device-under-test activity while setting up the analyzer.
Labels	Channels may be grouped together and given a 6-character name called a *label*. Up to 126 labels in each analyzer may be assigned with up to 32 channels per label. Trigger terms may be given an 8-character name.

Measurement Functions

Markers	Two markers (x and o) are shown as dashed lines in the display.
Time Intervals	The x and o markers measure the time interval between events occurring on one or more waveforms or states (available in state when time tagging is on).
Delta States	The x and o markers measure the number of tagged states between any two states (state only).
Patterns	The x or o marker can be used to locate the nth occurrence of a specified pattern before or after trigger. The o marker can also find the nth occurrence of a pattern before or after the x marker.

HP 1660E and 1670E-Series Logic Analyzer Specifications and Characteristics (cont.)

Statistics	x to o marker statistics are calculated for repetitive acquisitions. Patterns must be specified for both markers, and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum x to o time, maximum x to o time, average x to o time, and ratio of valid runs to total runs.
Compare Mode Functions	Performs post-processing bit-by-bit comparison of the acquired state data and compare image data.
Compare Image	Created by copying a state acquisition into the compare image buffer. Allows editing of any bit in the compare image to a 1, X or 0.
Compare Image Boundaries	Each channel (column) in the compare image can be enabled or disabled via bit masks in the compare image. Upper and lower ranges of states (rows) in the compare image can be specified. Any data bits that do not fall within the enabled channels and the specified range are not compared.
Stop Measurement	Repetitive acquisitions may be halted when the comparison between the current state acquisition and the current compare image is equal or not equal.
Compare Mode Displays	Reference Listing display shows the compare image and bit masks; difference listing display highlights differences between the current state acquisition and the compare image.

Data Display

Display Modes	State listing, state waveforms, state chart, state compare listing, compare difference listing, timing waveforms, timing listing, interleaved time-correlated listing of two state analyzers (time tags on), and time-correlated state listing with timing waveforms on the same display.
State X-Y Chart Display	Plots value of a specified label (on y-axis) versus states or another label (on x-axis). Both axes can be scaled.
State Waveform Display	Displays state acquisitions in waveform format.
Timing Listing Display	Displays timing acquisition in listing format.
Timing Waveform Display	
Accumulate	Waveform display is not erased between successive acquisitions.
Overlay Mode	Multiple channels can be displayed on one waveform display line. When waveform size is set to large, the value represented by each waveform is displayed inside the waveform in the selected base.
Displayed Waveforms	24 lines maximum on one screen. Up to 96 lines may be specified and scrolled through.
Bases	Binary, octal, decimal, hexadecimal, ASCII (display only), user-defined symbols, two's complement.
Symbols	
Pattern Symbols	User can define a mnemonic for the specific bit pattern of a label. When data display is "Symbol", mnemonic is displayed where the bit pattern occurs.
Range Symbols	User can define a mnemonic covering a range of values.
Symbol Utility	Symbolic information extracted from popular object module formats can also be used.
Number of Symbols	1000 maximum.
System Performance Analysis	SPA includes state histogram, state overview and time interval measurements to aid in the software optimization process. These tools provide a statistical overview of your synchronous design.

The HP 1664A Specifications and Characteristics

The HP 1664A is a low-cost version of the HP 1660E/ES/EP-series logic analyzer family. The HP 1664A has some specifications and characteristics that are different from the HP 1660E/ES/EP-series logic analyzers.

The HP 1664A:

- Supports a maximum of 50 MHz state acquisition
- Weight 26 pounds (11.8 kg)
- Altitude To 15,000 ft (4,752 m)
- Boots from the floppy disk drive—it does not have flash ROM
- It cannot be upgraded to include an oscilloscope or pattern generator
- The mouse and keyboard connectors are HP HIL standard
- For the optional keyboard order HP E2427A
- It does not support the symbol utility
- It does not support the software performance analysis (SPA) software
- It does not have a real time clock
- It does not have a hard disk drive
- It does not have a LAN port

HP 1660ES-Series Oscilloscope Specifications and Characteristics

General Information

Model Numbers	HP 1660ES, 1661ES, 1662ES, 1663ES
Number of Channels	2
Maximum Sample Rate	2 GSa/s per channel
Bandwidth [6] [10]	dc to 500 MHz (real time, dc coupled)
Rise Time [7] [10]	700 ps
Vertical Resolution	8 bits full scale
Memory Depth	32k samples

Oscilloscope Probing

Input Coupling	1 MΩ: ac,dc 50 Ω: dc only
Input R [10]	1MΩ ± 1% 50Ω ± 1%
Input C	~ 7pF
Probes Included	Two HP 1160A probes; 10:1, 10 MΩ, 9 pF 1.5 meters

Vertical (at BNC)

Maximum Safe Input Voltage	1 MΩ : ±250 V 50 Ω : 5 V rms
Vertical Sensitivity Range (1:1 Probe)	16 mV full scale to 40 V full scale
Probe Factors	Any integer ratio from 1:1 to 1000:1
Vertical (dc) Gain Accuracy [8]	± 1.25% of full scale
dc Offset Range (1:1 probe)	± 2V to ± 250V (depending on the vertical sensitivity)
dc Offset Accuracy [10]	± [1.0% of channel offset + 2.0% of full scale]
Voltage Measurement Accuracy [10]	± [1.25% of full scale + offset accuracy + 0.016 V/div]
Channel-to-Channel Isolation	dc to 50 MHz – 40 dB 50 MHz to 500 MHz – 30 dB

Horizontal

Time Base Range	0.5 ns/div to 5 s/div
Time Interval Measurement Accuracy [9] [10]	± [(0.005% of Δt) + ($2\times10^{-6}\times$ delay setting) + 150 ps]

Oscilloscope Triggering

Trigger Level Range	Bounded within channel display window
Trigger Sensitivity [10]	dc to 50 MHz: 0.063 × Full Scale 50 MHz to 500 MHz: 0.125 × Full Scale

Trigger Modes

Immediate	Triggers immediately after arming condition is met. (Arming condition is Run, Group Run, cross arming signal, or Port In BNC signal).
Edge	Triggers on rising or falling edge from channel 1 or 2.
Pattern	Triggers on entering or exiting logical pattern specified across channels 1 or 2. Each channel can be specified as high (H), low (L), or don't care (X) with respect to the level settings in the edge trigger menu. Patterns must be >1.75 ns in duration to be recognized.
Time-Qualified Pattern	Triggers on the exiting edge of a pattern which meets the user-specified duration criterion. Greater than, less than, or within range duration criterion can be used. Duration range is 20 ns to 160 ns. Recovery time after valid patterns with invalid duration is <12 ns.
Events Delay	Triggers on the nth edge or pattern as specified by the user. Time-qualification is applied only to the 1st of n patterns.
Auto-Trigger	Self-triggers if no trigger condition is found ~ 50 ms after arming.

Measurement Functions

Time Markers	Two markers (x and o) measure time intervals manually, or automatically with statistics.
Voltage Markers	Two markers (a and b) measure voltage and voltage differences.
Automatic Measurements	Period, frequency, rise time, fall time, +width, –width, peak-to-peak voltage, overshoot, and undershoot.

[6] Upper bandwidth reduces by 2.5 MHz for every degree C above 35°C.

[7] Rise time calculated as $t_r = \frac{0.35}{\text{bandwidth}}$

[8] Vertical gain accuracy decreases 0.08% per degree C from software calibration temperature.

[9] Specification applies at the maximum sampling rate. At lower rates, replace 150 ps in the formula with (0.15 × sample interval) where sample interval is defined as 1/sample rate.

[10] Specifications (valid within ± 10°C of auto-calibration temperature)

HP 1660EP-Series Pattern Generator Characteristics

Maximum memory depth	258,048 vectors
Number of output channels at 100 MHz to 200 MHz clock	16
Number of output channels at ≤100 MHz clock	32
Maximum number of "IF Condition" blocks at ≤50 MHz clock	1
Maximum number of different macros	100
Maximum number of lines in a macro	1024
Maximum number of parameters in a macro	10
Maximum number of macro invocations	1,000
Maximum loop count in a repeat loop	20,000
Maximum number of repeat loop invocations	1,000
Maximum number of Wait event patterns	4
Number of input lines to define a wait pattern	3
Maximum width of a label	32 bits
Maximum number of labels	126

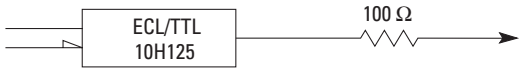
Lead Set Characteristics

HP 10474A 8-channel probe lead set	Provides most cost effective lead set for the HP 1660EP-series clock and data pods. Grabbers are not included.
HP 10347A 8-channel probe lead set	Provides 50 Ω coaxial lead set for unterminated signals, required for HP 10465A ECL Data Pod (unterminated). Grabbers are not included.

Data Pod Characteristics

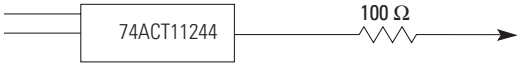
HP 10461A TTL DATA POD

Output type	10H125 with 100 Ω series
Maximum clock	200 MHz
Skew (note 1)	typical < 2 ns; worst case = 4 ns
Recommended lead set	HP 10474A



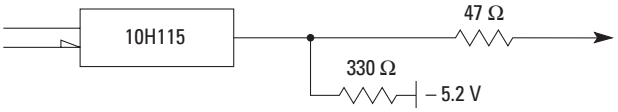
HP 10462A 3-STATE TTL/CMOS DATA POD

Output type	74ACT11244 with 100 Ω series; 10H125 on non 3-state channel 7 (note 2)
3-state enable	negative true, 100 KΩ to GND, enabled on no connect
Maximum clock	100 MHz
Skew (note 1)	typical < 4 ns; worst case = 12 ns
Recommended lead set	HP 10474A



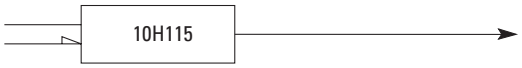
HP 10464A ECL DATA POD (TERMINATED)

Output type	10H115 with 330 Ω pulldown, 47 Ω series
Maximum clock	200 MHz
Skew (note 1)	typical < 1 ns; worst case = 2 ns
Recommended lead set	HP 10474A



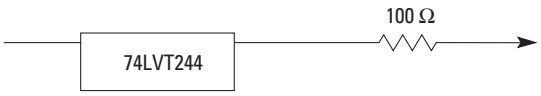
HP 10465A ECL DATA POD (UNTERMINATED)

Output type	10H115 (no termination)
Maximum clock	200 MHz
Skew (note 1)	typical < 1 ns; worst case = 2 ns
Recommended lead set	HP 10347A



HP 10466A 3-STATE TTL/3.3 VOLT DATA POD

Output type	74LVT244 with 100 Ω series; 10H125 on non 3-state channel 7 (note 2)
3-state enable	negative true, 100 KΩ to GND, enabled on no connect
Maximum clock	200 MHz
Skew (note 1)	typical < 3 ns; worst case = 7 ns
Recommended lead set	HP 10474A



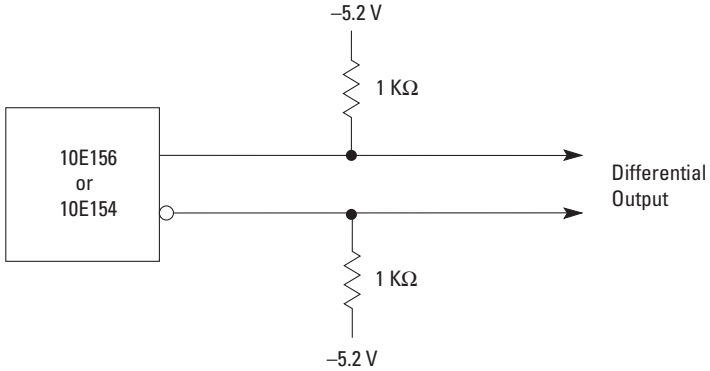
Note 1: Typical skew measurements made at pod connector with approximately 10 pF/50 KΩ load to GND; worst case skew numbers are a calculation of worst case conditions through circuits.

Note 2: Channel 7 on the 3-state pods has been brought out in parallel as a non 3-state signal. By looping this output back into the 3-state enable line, the channel can be used as a 3-state enable.

Data Cable Characteristics Without a Data Pod

The HP 1660EP data cables without a data pod provide an ECL terminated (1 KΩ to –5.2V) differential signal (from a type 10E156 or 10E154 driver). These are usable when received by a differential receiver, preferably with a 100 Ω termination across the lines. These signals should not be used single ended due to the slow fall time and shifted voltage threshold (they are not ECL compatible).

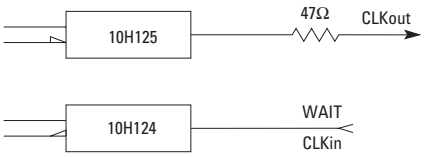
HP 1660EP Data Cable Output



Clock Pod Characteristics

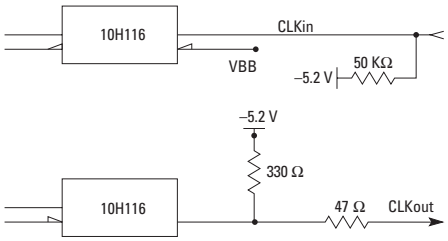
10460A TTL CLOCK POD

Clock output type	10H125 with 47 Ω series; true & inverted
Clock output rate	100 MHz maximum
Clock out delay	11 ns maximum in 9 steps
Clock input type	TTL – 10H124
Clock input rate	dc to 100 MHz
Pattern input type	TTL – 10H124 (no connect is logic 1)
Clock-in to clock-out	approximately 30 ns
Pattern-in to recognition	approx. 15 ns + 1 clk period
Recommended lead set	HP 10474A



10463A ECL CLOCK POD

Clock output type	10H116 differential unterminated; and differential with 330 Ω to –5.2V and 47 Ω series
Clock output rate	200 MHz maximum
Clock out delay	11 ns maximum in 9 steps
Clock input type	ECL – 10H116 with 50 KΩ to –5.2v
Clock input rate	dc to 200 MHz
Pattern input type	ECL – 10H116 with 50 KΩ (no connect is logic 0)
Clock-in to clock-out	approximately 30 ns
Pattern-in to recognition	approx. 15 ns + 1 clk period
Recommended lead set	HP 10474A



Probing Alternatives for the HP 1660E/ES/EP and 1670E-Series Logic Analyzers

Probing the device under test is both one of the potentially most difficult and certainly one of the most important tasks in debugging a digital design. That is why HP provides a wider variety of probing solutions than anyone else in the industry—each with a different set of advantages particular to a given situation. We like to think of it as helping you get your signals off to a great start.

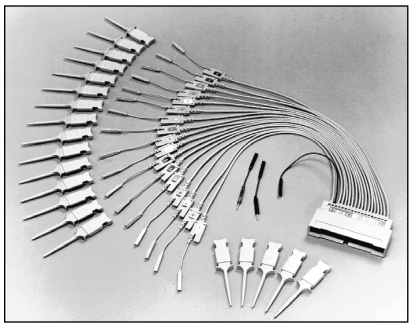


Figure 5. General-purpose lead sets

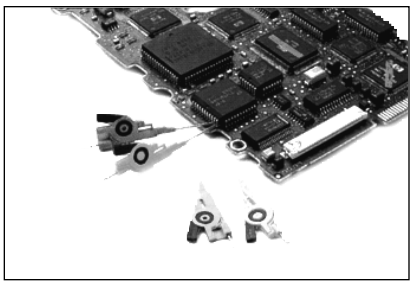


Figure 6. Ultra-fine pitch surface mount device clips

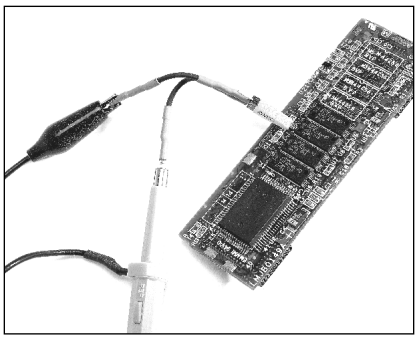


Figure 7. HP Wedge probe adapters for QFP package

Probing Alternative	Advantages	Limitations
General Purpose Lead Sets and Surface Mount Grabbers	Most flexible method. Works in conjunction with SMD clips and Wedge adapters listed below. Included with logic analyzer purchase.	Can be cumbersome when connecting a large number of channels
Ultra-Fine Pitch Surface Mount Device Clips	Smallest IC clips in the industry to date (down to 0.5 mm). Works with both logic analyzer and scope probing systems.	Same as above plus small incremental cost
HP Wedge probe adapter for QFP Packages	Compressible dual conductors between adjacent IC legs make 3-8 adjacent signal leads available to logic analyzer and scope probing systems.	Same as above plus small incremental cost
Elastomeric and Locator Base Solutions for Generic QFP Packages	Provides access to all signal leads for generic QFP packages (including custom ICs). Uses combination of one probe adapter and four flexible adapters, plus general-purpose lead sets.	Requires minimal keep out area. Moderate to significant incremental cost.
Direct Connection to Device Under Test via Built-In Connectors	Very reliable and convenient probing system when frequent probing connections are required (mfg. or field test for example). Connectors can be located at optimal position in the device under test. Can work in conjunction with HP provided inverse assemblers.	Requires advance planning to integrate into design process. Moderate (normal density) to significant (high density) incremental cost.
HP Analysis Probes for Specific Processors and Buses	Support for over 200 different processors and buses. Includes reliable logic analyzer probe pod connectors, logic analyzer configuration files and device specific inverse assemblers.	Requires moderate clearance around processor or bus. Moderate to significant extra cost depending on specific processor or bus.

HP Wedge Probe Adapter

IC leg spacing	Number of signals	Number of Wedges in pack	HP model number
0.5 mm	3	1	HP E2613A
0.5 mm	3	2	HP E2613B
0.5 mm	8	1	HP E2614A
0.65 mm	3	1	HP E2615A
0.65 mm	3	2	HP E2615B
0.65 mm	8	1	HP E2616A

Probing Solutions

Package type	Pin Pitch	Elastomeric solutions	Locator base solutions
304-pin PQFP/CQFP	0.5 mm		HP E5331A probe adapter HP E5333A flexible adapter
240-pin PQFP/CQFP	0.5 mm	HP E5363A probe adapter HP E5371A 1/4-flexible adapter	HP E5315A probe adapter HP E5316A flexible adapter HP E5330A rigid adapter
208-pin PQFP/CQFP	0.5 mm	HP E5374A probe adapter HP E5371A 1/4-flexible adapter	HP E5318A probe adapter HP E5316A flexible adapter HP E5330A rigid adapter
184-pin PQFP/CQFP	0.5 mm		HP E5343A probe adapter HP E5316A flexible adapter HP E5330A rigid adapter
176-pin PQFP	0.5 mm	HP E5348A probe adapter HP E5349A 1/4-flexible adapter	
160-pin QFP	0.5 mm	HP E5377A probe adapter HP E5349A 1/4-flexible adapter	
160-pin PQFP/CQFP	0.65 mm	HP E5373A probe adapter HP E5349A 1/4-flexible adapter	HP E5319A probe adapter HP E5316A flexible adapter HP E5330A rigid adapter
144-pin PQFP/CQFP	0.65 mm	HP E5361A probe adapter HP E5340A 1/4-flexible adapter	
144-pin TQFP	0.5 mm	HP E5336A probe adapter HP E5340A 1/4 flexible adapter	

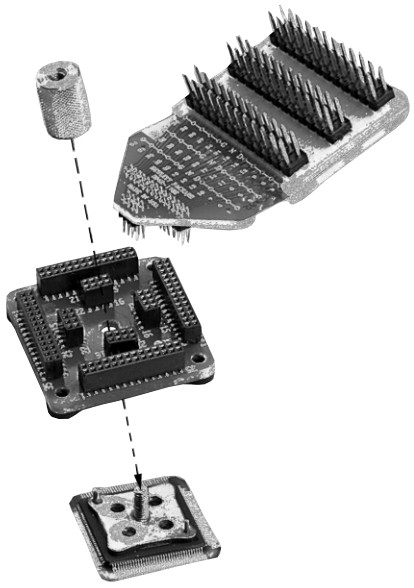


Figure 8. Elastomeric probing solution

HP Analysis Probes for Specific Processors and Buses

Please see *Processor and Bus Support for HP Logic Analyzers* (pub. no. 5966-4365E) for detailed information and ordering instructions for HP Analysis Probes. This document also contains additional and up to date information on the other probing alternatives described previously.

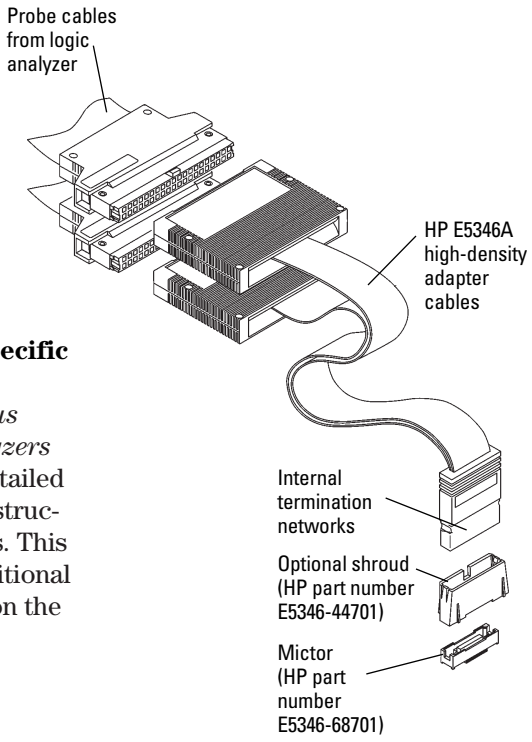


Figure 9. High density direct connection solution

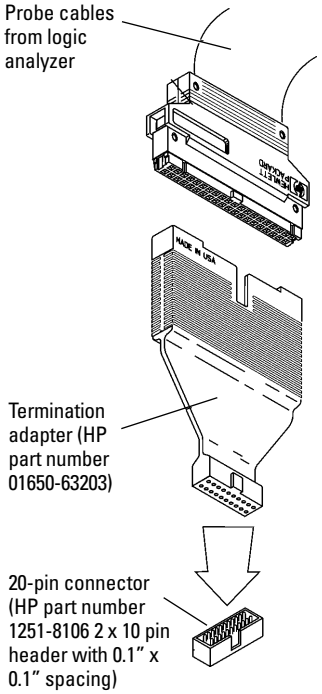


Figure 10. Normal density direct connection solution

Accessories for the HP 1660ES Series Logic Analyzers

Oscilloscope Probes

HP 1160 Family of Miniature Passive Probes

The HP 1160 family of miniature probes was developed as a result of intensive market research on probing. We developed a probe with a browser that won't slip off the test point being probed and short to some adjacent point. The browser uses a crown point that digs into solder, and won't slip. These probes include a variety of ground leads and 50 mil SMD clips for attaching to different grounding points. Each HP 1660ES series logic analyzer ships with the HP 1160 family passive probes.

Each HP 1160 family probe includes:

- 1 probe assembly
- 1 general-purpose retractable hook tip
- 1 browser
- 2 barrel insulators
- 4 spring grounds
- 1 alligator ground lead
- 1 socketed ground lead
- 1 dual lead adapter
- 2 SMD grabbers
- 1 spare browser pogo pin
- 1 spare probe tip
- 1 screwdriver
- 1 users' reference
- 3-year warranty

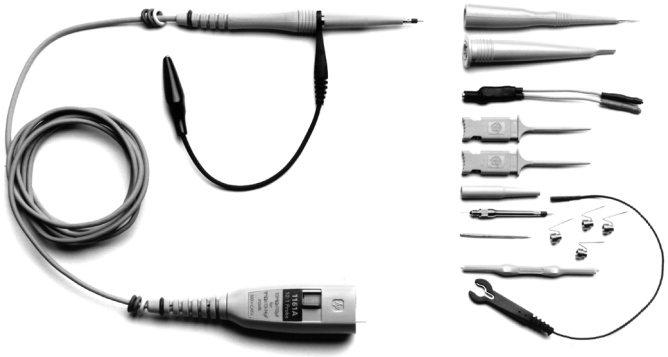


Figure 11. HP 1160 probes and accessories

Figure 12. HP 1182A standard testmobile

Figure 13. HP 1184A deluxe testmobile

HP 1660E/ES/EP Series Ordering Information

HP 1660E/ES/EP and 1670E Series Benchtop Logic Analyzers

HP 1660E	136 Channel Color Logic Analyzer
HP 1661E	102 Channel Color Logic Analyzer
HP 1662E	68 Channel Color Logic Analyzer
HP 1663E	34 Channel Color Logic Analyzer
HP 1660ES	136 Channel Color Logic Analyzer with 2 channel, 500 MHz oscilloscope
HP 1661ES	102 Channel Color Logic Analyzer with 2 channel, 500 MHz oscilloscope
HP 1662ES	68 Channel Color Logic Analyzer with 2 channel, 500 MHz oscilloscope
HP 1663ES	34 Channel Color Logic Analyzer with 2 channel, 500 MHz oscilloscope
HP 1660EP	136 Channel Color Logic Analyzer with 32 channel, 100 Mvectors/sec pattern generator
HP 1661EP	102 Channel Color Logic Analyzer with 32 channel, 100 Mvectors/sec pattern generator
HP 1662EP	68 Channel Color Logic Analyzer with 32 channel, 100 Mvectors/sec pattern generator
HP 1663EP	34 Channel Color Logic Analyzer with 32 channel, 100 Mvectors/sec pattern generator
HP 1670E	136 Channel Color Logic Analyzer with 1M deep acquisition memory
HP 1671E	102 Channel Color Logic Analyzer with 1M deep acquisition memory
HP 1672E	68 Channel Color Logic Analyzer with 1M deep acquisition memory
HP 1664A	34 Channel Monochrome Logic Analyzer

HP 1660E/ES/EP Series and HP 1670E Series Product Options

Opt OB1	Additional User Manual
Opt OB3	Add Service Manual
Opt OBF	Add Programming Manual
Opt ICM	Rack Mount Kit
Opt IBP	MilStd 45662 Calibration
Opt ABJ	Japanese localization of user manual
Opt UK9	Front Panel Cover
Opt W30	3-year extended repair service
Opt W50	5-year extended repair service

HP 1660EP Series Product Options for the Pattern Generator

At least one clock pod and lead set must be ordered for the pattern generator of the HP 1660EP Series. Also, order a data pod for every eight output channels used. There is a total of one clock pod and four data pods on each HP 1660EP series pattern generator.

011	TTL Clock Pod and Lead Set
012	Tri-State TTL/3.3V Data Pod and Lead Set
013	Tri-State TTL/CMOS Data Pod and Lead Set
014	TTL Data Pod and Lead Set
021	ECL Clock Pod and Lead Set
022	ECL (terminated) Data Pod and Lead Set
023	ECL (unterminated) Data Pod and Lead Set

HP 1660E/ES/EP Series Ordering Information (Cont.)

Probing Alternatives for HP Benchtop Logic Analyzers

HP 10467-68701	0.5 mm SMD clips (Qty 4)
HP E2613A	HP Wedge, 0.5mm, 3 signal (Qty1)
HP E2613B	HP Wedge, 0.5mm, 3 signal (Qty 2)
HP E2614A	HP Wedge, 0.5mm, 8 signal (Qty 1)
HP E2615A	HP Wedge, 0.65mm, 3 signal (Qty1)
HP E2615B	HP Wedge, 0.65mm, 3 signal (Qty 2)
HP E2616A	HP Wedge, 0.65mm, 8 signal (Qty. 1)
HP E5346A	High Density Termination Adapter
HP E5346-44701	Shroud for High Density T.A.
HP E5346-68701	Mictor High Density Connector (Qty 5)
HP 01650-63203	Normal Density Termination Adapter
HP 1251-8106	Normal Density 20-pin Connector

Optional Oscilloscope Probes for HP 1660ES Series Logic Analyzers

HP 1145A	2 Channel, 750 MHz Active Probes
HP 1142A	External Power Supply for HP 1145

Testmobiles for HP Benchtop Logic Analyzers

HP 1182A	Standard Testmobile
HP 1184A	Deluxe Testmobile

Accessories for HP Benchtop Logic Analyzers

HP E2427B	DIN (PC-Style) Keyboard
HP E2427A	HIL Keyboard (HP 1664A only)
HP 1540-1066	Soft Carrying Case
HP 5062-7379	Rack Mount Kit (same as option ICM)

HP 1660E Series Post Purchase Upgrades

The following two upgrades can be added to an HP 1660E Series logic analyzer at a later date if the additional functionality is desired.

HP E2460ES	Upgrade to add two-channel, 500-MHz bandwidth, 2-GSa/s, 32k memory oscilloscope to an HP 1660E Series model
HP E2495A	Upgrade to add thirty-two channel, 100 MVectors/sec, 256k memory pattern generator to an HP 1660E Series model

Replacement Part Numbers for Logic Analyzer Probes

HP 5959-9333	Five gray probe leads
HP 5959-9334	Five short ground leads
HP 01650-61608	16-Channel probe lead set
HP 5090-4356	Surface-mount grabbers (package of 20)
HP 5959-0288	Throughhole grabbers (package of 20)

Replacement Model Numbers for Pattern Generator Probing

As a convenience, the individual model numbers for the HP 1660EP series pattern generator clock/data pods and lead sets are listed here. Normally these are ordered as product options at the time of purchase. They are listed here for any future needs that may arise.

HP 10460A	TTL Clock Pod for the HP 1660EP-Series
HP 10461A	8-channel TTL Data Pod for the HP 1660EP-Series
HP 10462A	8-channel 3-state TTL/CMOS Data Pod for the HP 1660EP-Series
HP 10463A	ECL Clock Pod for the HP 1660EP-Series
HP 10464A	8-channel ECL (terminated) Data Pod for the HP 1660EP-Series
HP 10465A	8-channel ECL (unterminated) Data Pod for the HP 1660EP-Series (use HP 10347A lead set)
HP 10466A	8-channel 3-state TTL/3.3V Data Pod for the HP 1660EP-Series
HP 10474A	8-channel Probe Lead Set for the HP 1660EP-Series
HP 10347A	8-channel (50-ohm Coaxial) Probe Lead Set

Related HP Literature

Title	Publication Description	HP Pub. Number
Logic Analysis and Emulation Solutions Version 3.0	CD-Rom	5965-7502E
Processor and Bus Support for HP Logic Analyzers	Configuration Guide	5966-4365E

Warranty Information

All Hewlett-Packard products described in this document are warranted against defects in material and workmanship for a period of one year from date of shipment. Three-year and five-year return-to-HP repair services are also available. Refer to individual product manuals for detailed descriptions and terms of warranty. As an added benefit to HP 1664A customers, this product comes standard with a three-year return to HP warranty.

For more information about Hewlett-Packard test and measurement products, applications and services, visit our web site: http://www.hp.com/go/tmdir.
For more information on HP 1660 and 1670E-Series benchtop logic analyzers, visit our website: http://www.hp.com/go/benchtopLA.
You can also contact one of the following centers and ask for a test and measurement sales representative. If you plan to purchase a new logic analyzer within the next 3 months and have budget approved for the purchase, HP can arrange for you to test drive a unit.

United States:
Hewlett-Packard Company
Test and Measurement Call Center
P.O. Box 4026
Englewood, CO 80155-4026
1 800 452 4844

Canada:
Hewlett-Packard Canada Ltd.
5150 Spectrum Way
Mississauga, Ontario
L4W 5G1
(905) 206 4725

Europe:
Hewlett-Packard
European Marketing Centre
P.O. Box 999
1180 AZ Amstelveen
The Netherlands
(31 20) 547 9900

Japan:
Hewlett-Packard Japan Ltd.
Measurement Assistance Center
9-1, Takakura-Cho, Hachioji-Shi,
Tokyo 192-8510, Japan
(81) 426 56 7832

Latin America:
Hewlett-Packard
Latin American Region Headquarters
5200 Blue Lagoon Drive
9th Floor
Miami, Florida 33126
U.S.A.
(305) 267 4245/4220

Australia/New Zealand:
Hewlett-Packard Australia Ltd.
31-41 Joseph Street
Blackburn, Victoria 3130
Australia
1 800 629 485 (Australia)
0 800 738 378 (New Zealand)

Asia Pacific:
Hewlett-Packard Asia Pacific Ltd
17-21/F Shell Tower, Times Square,
1 Matheson Street, Causeway Bay,
Hong Kong
(852) 2599 7777

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5968-0327E **11/98**
Printed in the U.S.A.