1.5 Specifications

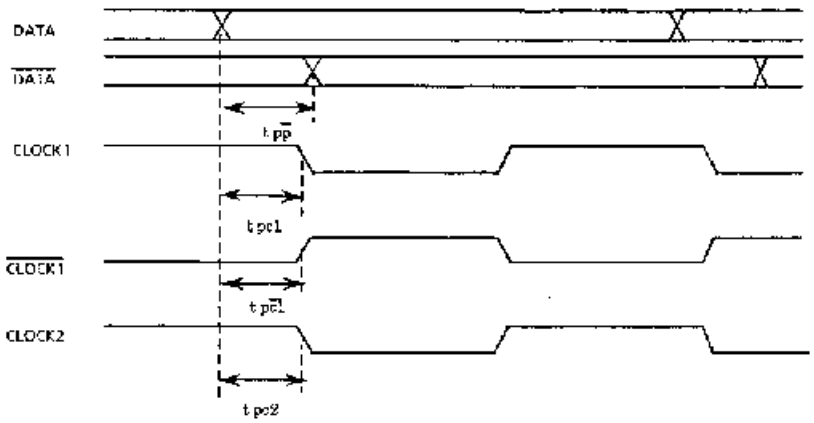
Operation frequency range	Internal clock		0.05 to 10 GHz		
	External clock		0.05 to 10 GHz		
External clock	Input level		0.7 to 2.0 Vp-p		
	Waveform		0.05 to 0.5 GHz: square wave (duty factor: 50%) >0.5 GHz: sinusoidal or square wave (duty factor: 50%)		
	Connector		APC 3.5 (with female to female adaptor)		
Internal clock	Frequency range		0.05 to 10 GHz		
	Resolution		1 kHz, 1 MHz		
	Frequency accuracy		±1 ppm		
	SSB phase noise		At 10 kHz offset ≦-85 dBc/Hz (0.05 to <4.0 GHz) ≦-80 dBc/Hz (4.0 to <8.0 GHz) ≦-75 dBc/Hz (8.0 to 10 GHz)		
	Reference signal		10 MHz (INT/EXT selectable)		
Pattern generation	Pseudorandom binary sequence pattern (PRBS)	Pattern length	2^N-1: N = 7, 9, 11, 15, 20, 23, 31		
		Mark ratio	1/2, 1/4, 1/8, 0/8 (1/2, 3/4, 7/8, 8/8 also possible by logic inversion)		
		Number of "AND bit" shifts when setting mark ratio	1 bit or 3 bit (Selectable using rear panel DIP switch)		
	DATA pattern	Data length	2 to 524288 bits	Data length	Step width
				2 to 4096	1 step 524288/128 = 4096
				4224 to 524288	128 step 128N (N = 33 to 4096)
		Pattern reset/preset	ALL/PAGE selectable		

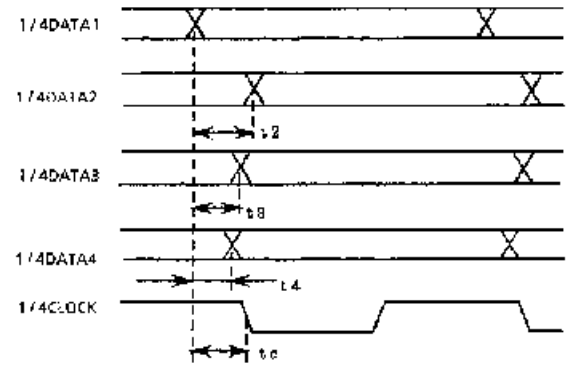
Pattern generation (Cont.)	Word pattern	Word length	2 to 16 bits
		Number of words	1 to 32768
		Pattern reset/preset	ALL/PAGE selectable

Relationship between Word Length and Number of Words

Word length N	Number of Words			
	Range	Step width	Range	Step width
2	1 to 2048	1 step	2112 to 32768	64 step
3	1 to 1365	1 step	1408 to 32768	128 step
4	1 to 1024	1 step	1056 to 32768	32 step
5	1 to 819	1 step	896 to 32768	128 step
6	1 to 682	1 step	704 to 32768	64 step
7	1 to 585	1 step	640 to 32768	128 step
8	1 to 512	1 step	528 to 32768	16 step
9	1 to 455	1 step	512 to 32768	128 step
10	1 to 409	1 step	448 to 32768	64 step
11	1 to 372	1 step	384 to 32768	128 step
12	1 to 341	1 step	352 to 32768	32 step
13	1 to 315	1 step	384 to 32768	128 step
14	1 to 292	1 step	320 to 32768	64 step
15	1 to 273	1 step	384 to 32768	128 step
16	1 to 256	1 step	264 to 32768	8 step

Pattern generation (Cont.)	External pattern input mode	Number of channels	8 CH (1 to 8 CH input settings are possible)
		Pattern bit rate	1/8 speed of fundamental clock
		Clock output *1	ECL, 50 Ω, connected with −2 V *1 Output of clock for external 1/8 pattern generation
		External pattern input level	ECL, 50 Ω, connected with −2 V
		Connector	SMA
	Logic inversion		possible
	Error insertion	Error rate	10^{-n}: n = 4, 5, 6, 7, 8, 9 and single
		Insertion position	possible to insert into any 1 CH of 32 CH (Selectable with rear panel switch)
DATA output	Waveform format		NRZ
	Number of outputs		2 (DATA/$\overline{\text{DATA}}$)
	(DATA/$\overline{\text{DATA}}$) tracking mode		ON/OFF selectable
	Amplitude		0.5 to 2 Vp-p, variable in 10 mV steps [Setting error: ≦ ±15%, ±100 mV whichever is greater]
	Offset voltage		Voltage: −2 to +2 V (V_{OH}), variable in 5 mV steps [Setting error: ≦ ±15%, ±100 mV or ±15% of amplitude whichever is greatest] Display mode: V_{OH}, V_{TH}, V_{OL}, selectable
	Rise/fall time		≦ 30 ps
	Pattern jitter		≦ 25 ps
	Crosspoint adjust function		DATA, $\overline{\text{DATA}}$, adjustable, independently
	Waveform distortion		<10% or <100 mV, whichever is greater
	Load impedance		50 Ω (with back termination)
	Connector		APC 3.5 (with female to female adaptor)

CLOCK output	Number of outputs	3 (CLOCK 1, $\overline{\text{CLOCK 1}}$, CLOCK 2)
	CLOCK 1, $\overline{\text{CLOCK 1}}$ delay	±500 ps, variable in 1 ps steps
	CLOCK 1, $\overline{\text{CLOCK 1}}$ amplitude	0.5 to 2 Vp-p, variable in 10 mV steps [Setting error: ≤ ±15% or ±100 mV whichever is greater]
	CLOCK 2 amplitude/offset voltage	2 Vp-p (≦ ±15%) fixed/0 V (≤ ±300 mV) fixed
	Offset voltage	Voltage: −2 to +2 V (V_{OH}), variable in 5 mV steps [Setting error: ≤ ±15%, ±100 mV or ±15% of amplitude whichever is greatest] Display mode: V_{OH}, V_{TH}, V_{O_S} selectable
	Rise/fall time	Of 20% to 80% amplitude: ≦ 30 ps (≧ 5 GHz) ≤ 50 ps (< 5 GHz)
	Waveform distortion	<10% or 100 mV whichever is greater
	Duty ratio adjust function	Of CLOCK 1, $\overline{\text{CLOCK 1}}$ and CLOCK 2, adjustable independently
	Load impedande	50 Ω (with back termination)
	Connector	APC 3.5 (with female to female adaptor)
Output phase	 $\lvert t_{p\overline{p}} \rvert \leq 30$ ps $\lvert t_{pc1} \rvert \leq 30$ ps $\lvert t_{p\overline{c}1} \rvert \leq 30$ ps $\lvert t_{pc2} \rvert \leq 30$ ps Where CLOCK1/$\overline{\text{CLOCK1}}$ delay is set to 0ps.	

1/4 DATA/ CLOCK output	Number of outputs	DATA: 4 CLOCK: 1
	Output level	0.5 to 1 Vp-p, variable in 10 mV steps [Setting error : ≦ ± 15% or ± 100 mV whichever is greater]
	Offset voltage	Voltage: − 1.5 to + 1.5 V (V_{OH}), variable in 5 mV steps [Setting error : ≦ ± 150 mV] Display mode : V_{OH}, V_{IH}, V_{OL}, selectable
	Rise/fall time	Of 20% to 80% amplitude ≦ 200 ps
	DATA output jitter	≦ 100 ps
	Waveform distortion	≦ 15%
	Skew	 | t2 | ≦ 100ps | t3 | ≦ 100ps | t4 | ≦ 100ps | te | ≦ 100ps
	Connector	SMA

Sync signal output	Number of outputs	Pattern : 1 (BNC connector) 1/2 CLOCK: 1 (SMA connector) 1/32 CLOCK: 1 (BNC connector)
	Output level	1 Vp-p ± 20% (VoH: 0 V, < ± 200 mV)/50 Ω
External control		GP-IB (IEEE 488.2)
Ambient temperature, rated range of use		0° to 50°C (However, 5° to45°C applied for pattern memory floppy disk)
Parameter memory	Media	3.5 inch floppy disk (2HD) 1.6 Mbyte (unformat)
	Format	MS-DOS, Rev. 3.1
	Content	Programmable pattern and other parameters
Power		**Vac ± 10% (max. 250 Vac), 48 ~ 63 Hz, ≦ 700 VA
Dimensions and weight		221H x 426W x 450D mm, <33 kg