

quantumdata™ 980

DisplayPort 1.4 / USB-C / eDP

Video Generator / Protocol Analyzer

Video Generation and Analysis

Testing up to 8.1 Gb/s Link Rates

Link, FEC & DSC Compliance Suites now Approved!



Key Features

- Run DisplayPort functional tests and protocol compliance tests up to full DP 1.4 specification
- Equipped with both DP standard and USB-C ports for Tx and Rx function—all test features supported through either type of connector
- View Power Delivery (PD) negotiations for USB-C DP Alt Mode
- Run functional tests on displays and monitors up to 8.1 Gb/s link rates with large format and test pattern library
- Generate Display Stream Compression (DSC) select patterns and configure slices and video parameters
- Configure link training parameters to test display's handling
- View EDID and DPCD registers
- Access DSC Test CRC registers for automated verification of source DSC compression
- Test DP sources up to 8.1 Gb/s link rates; view incoming video and meta-data—including DSC compressed—from a source device in real time
- Capture and decode incoming video, protocol and control packets—including Display Stream Compression (DSC)
- **UPDATE!** Run DP 1.4 EDID compliance tests on sink devices
- Monitor Aux Channel transactions as a DP source or sink
- Passively monitor Aux Channel between a source & display even at 8.1Gb/s link rates
- Run DP 1.4 Link Layer compliance tests on sources and sinks up to 8.1 Gb/s link rates
- **NEW!** Run DP 1.4 EDID compliance tests on sinks
- Run DP 1.4 Forward Error Correction (FEC) compliance tests
- Run DP 1.4 Display Stream Compression compliance tests for sources and sinks
- Run DCP-approved HDCP 2.2 compliance tests on DisplayPort sources, sinks and repeaters
- Run audio tests using programmable LPCM sine wave audio tones and compressed formats
- Run tests on embedded DisplayPort (eDP) 1.4b sources and panels using fast link training and ALPM
- Test eDP backlight control functions on panel using either backlight control pins or Aux Channel control commands

The Teledyne LeCroy quantumdata 980 DP1.4/USB-C/eDP Video Generator/ Analyzer module provides an unprecedented combination of functional and compliance testing for video, audio and protocol of DisplayPort devices. The module supports 1.62, 2.7, 5.4 & 8.1 Gb/s data rates on 1, 2 & 4 lanes on its Tx video generator port and its Rx analyzer port for both the standard DP ports and the new USB-C ports with DP Alt Mode.

The module's protocol analyzer supports real time analysis and deep analysis using captures of incoming DisplayPort streams from source devices including DSC/FEC compressed streams. The module's video generator can be used for testing displays, USB-C adapters, extenders, etc. The module is equipped with all the standard video timings and test patterns necessary for testing modern displays.

The 980 DP 1.4 Video Generator / Protocol Analyzer module supports a full suite of link layer and **NEW!** EDID compliance tests for both sources and sinks including compliance tests for forward error correction (FEC).

The full-size DP and USB-C Tx and Rx ports support Auxiliary Channel analysis of the DP Aux Channel, and the USB-C ports support Aux Channel Analysis of the USB-C Configuration Channel. An included Aux Chan monitoring board supports passive monitoring of the DP aux channel via full-size DisplayPort connectors, between a source and display. This enables analysis of link training and HDCP interoperability between devices.

For developers of Embedded DisplayPort (eDP), the new module offers the hardware necessary to support a variety of optional eDP features. Initial support includes fast link training, alternate scrambler seed, Advanced Link Power Management (ALPM) and Tx backlight control. A pin header is available to provide access to the backlight Tx control test feature.

The module can be equipped in the 980B Test Platform and controlled either through the embedded 980 GUI Manager or the PC-based GUI Manager

Source Testing

The 980 DP 1.4 Video Generator / Analyzer module emulates a DP display device (sink) for analyzing source devices. There are two options for the analysis function for testing DisplayPort source devices:

- Basic Analyzer – Provides real time viewing of video and metadata for functional testing.
- Capture/Store Protocol Analyzer – Provides capture and store of the main link including protocol and control packets, main stream attributes and secondary data.

Display Testing

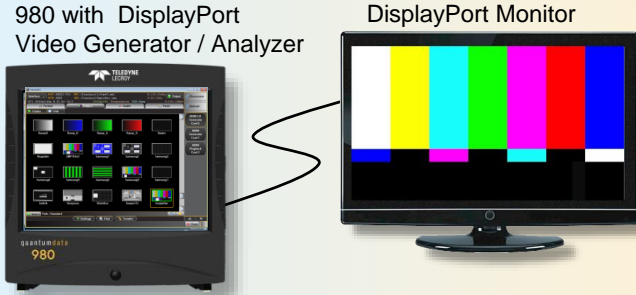
The 980 DP 1.4 Video Generator / Analyzer module supports video, audio and protocol functional testing of high-end DP displays. The module supports 1.62, 2.7, 5.4 & 8.1 Gb/s data rates on 1, 2 & 4 lanes on both its Tx ports and its Rx ports.

The module also supports DP 1.4 Link Layer HDCP 2.2 compliance testing for DisplayPort source, sink and repeater devices and link layer compliance testing for sink devices.

DISPLAY TESTS – VIDEO/AUDIO TESTING

Video Generation

The 980 DP 1.4 Video Generator / Analyzer module supports video and audio functional testing at link rates up to 8.1 Gb/s on 1, 2 and 4 lanes to support high resolution formats. The module has an extensive set of video formats and library of test patterns. You can set any pattern in motion to test motion artifacts with the Image Shift feature.



Test Setup for Sink Test

Link Training Control and Configuration

The module's link training control feature enables you to configure the link training parameters during testing. You can set limits on the lane count and link rate and allow the link training engine to establish link training based on those limitations or you can force link training parameters—lane count, link rate, voltage swing, pre-emphasis.

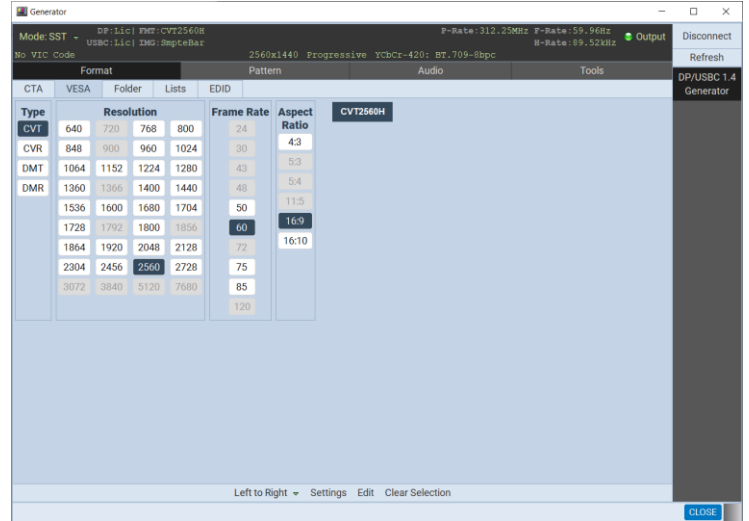
Link Training Control and Configuration



Alt Mode Negotiation

The USB Type C Transmit connector participates in discovery, power contract negotiation, and DP Alt Mode negotiation. The protocol messages can be monitored on the Auxiliary Channel Analyzer (right).

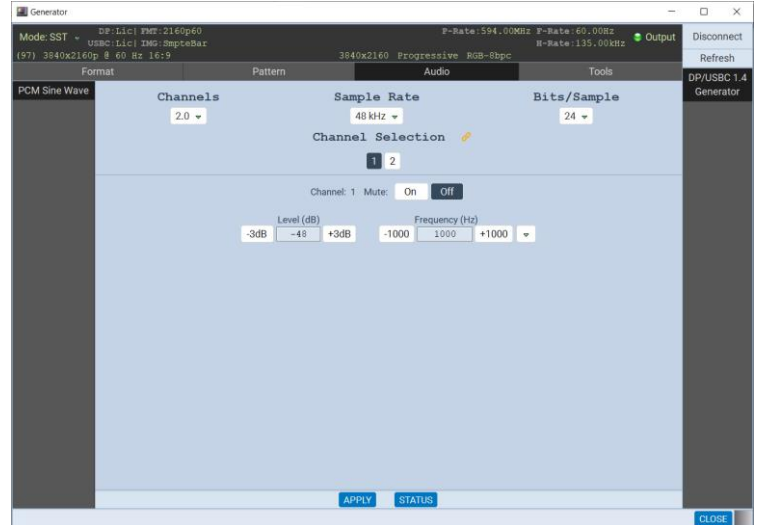
Format Selection



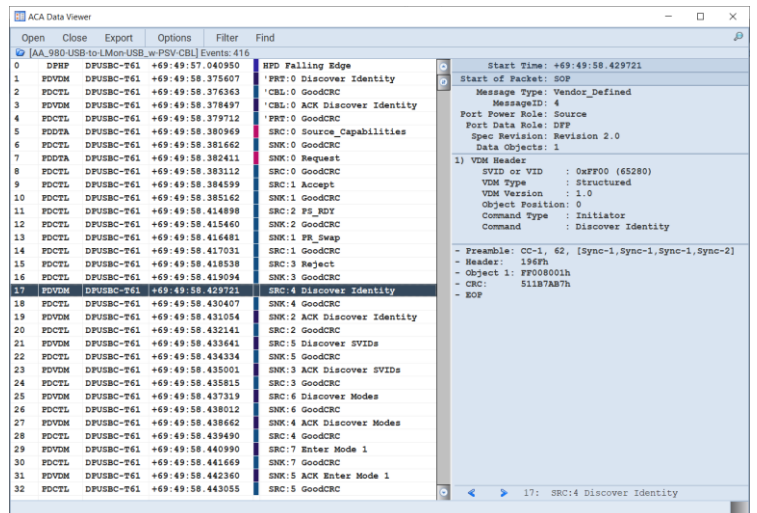
Audio Testing

The module offers a programmable LPCM audio sine wave generator enabling you to set the number of channels (up to 8), the amplitude, frequency, sampling rate and bit depth for uncompressed formats.

LPCM Audio Testing



Aux Channel Analyzer – DP Alt Mode Negotiation



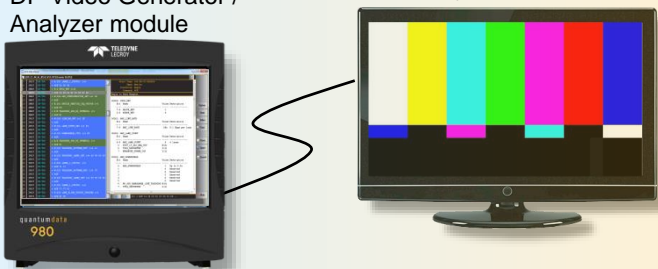
DISPLAY TESTS - PROTOCOL TEST FEATURES

Protocol Testing

The 980 DP 1.4 Video Generator / Analyzer module offers a variety of features for testing DisplayPort protocols. You can verify HDCP 1.3 and HDCP 2.2 authentication transactions between the module's Tx port and a DP display. The module's EDID Decode feature enables you to examine the EDID of the connected display. The DPCD Decode feature enables you to examine the DPCD registers of the connected display. You can read the EDID and/or the DPCD of downstream MST nodes.

980 with
DP Video Generator /
Analyzer module

DisplayPort Monitor



Test Setup for Sink Test

Multi-Stream Transport

The DP 1.4 Video Generator / Analyzer module emulates an MST source for testing an MST branch device or MST-capable monitor. Up to four (4) streams are supported with a depth of one. The Auxiliary Channel Analyzer (ACA) utility depicts the MST negotiations with the connected MST Rx device.

Auxiliary Channel Analyzer

The 980 DP 1.4 Video Generator / Analyzer module's Auxiliary Channel Analyzer (ACA) feature enables you to monitor the DP Aux Channel for link training and MST negotiations, HDCP transactions and EDID exchanges between the DP 1.4 module and a connected display. The ACA logs these events and assigns precise timestamps to them. You can view the details of each transaction. These ACA logs can be saved and disseminated for further analysis by colleagues and other subject matter experts.

Aux Channel Analyzer – Link Training

Bit Name	Value	Description
0	0	Reserved
1	0	Reserved
2	0	Reserved
3	0	Reserved
4	0	Reserved
5	POST_LINK_TRAINING	N(0)
6	TP23_SUPPORTED	Y(1)
7	ENHANCED_FRAME_CAP	Y(1)

EDID Decode View

Manufacturer: Q01
Product Code: 903 (03D4h)
Serial #: 17 (0000011h)
Model Year: 2017
EDID Version 1, Revision 4
Number of additional blocks: 1

DPCD Register View

Bit Name	Value	Description
0	0	Reserved
1	0	Reserved
2	0	Reserved
3	0	Reserved
4	0	Reserved
5	NO_AUX_HANDSHAKE_LINK_TRAINING	N(0)
6	TP23_SUPPORTED	Y(1)
7	TP24_SUPPORTED	Y(1)

HDCP 2.2 Test

HDCP Mode: None, 1.3, 2.3
Key Type: Production, Facsimile
Status: AUTHENTICATED YES

SOURCE TESTS – CAPTURE & DECODE FOR DEEP

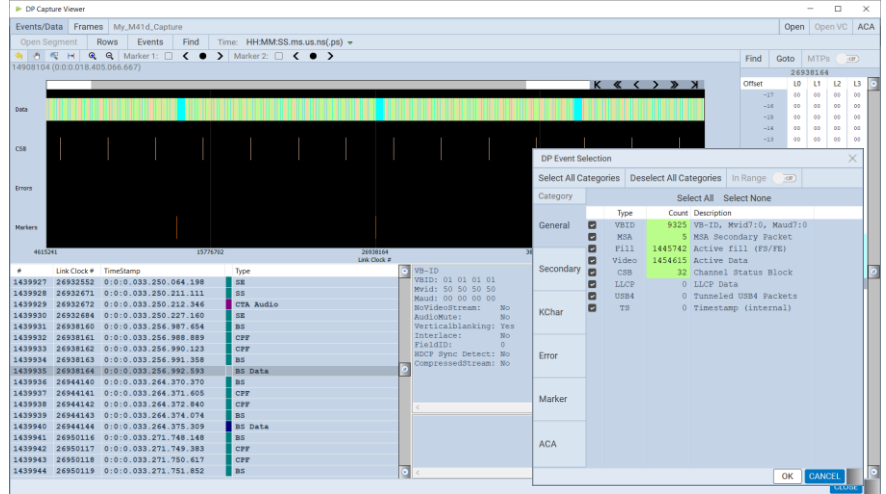
Capture and Decode

The 980 DP 1.4 USB-C Video Generator / Analyzer captures and decodes the main link attributes in order to diagnose interoperability issues related to them. The Protocol Analyzer captures & stores main link data and provides visibility into main stream attributes, secondary data elements, K-Characters and protocol errors. The Protocol Analyzer presents these elements on a graphical timeline and in a table. You can search for data and select any transaction in the table to view its details. The capture utility also enables you to capture specific MST streams from the source.

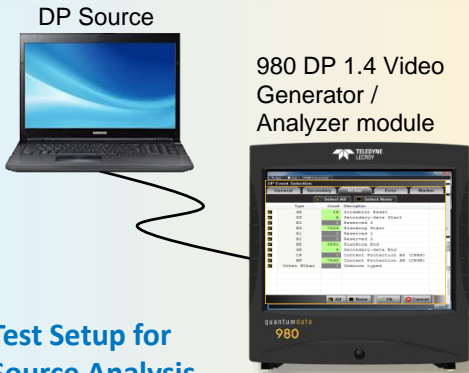
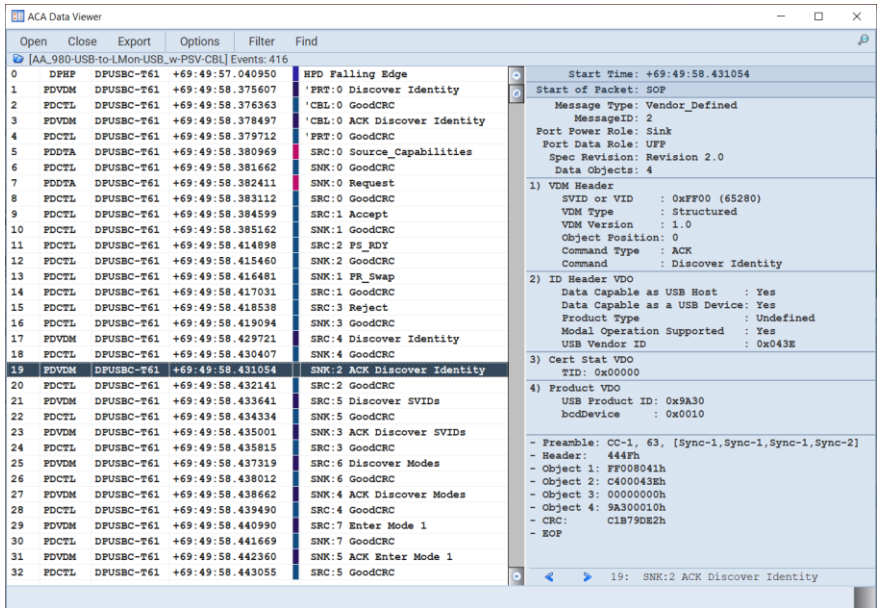
DP Alt Mode Negotiation

The 980 DP 1.4 USB-C Generator / Analyzer USB-C Rx connector participates in discovery, power contract negotiation, and DP Alt Mode negotiation. The protocol messages can be monitored on the Auxiliary Channel Analyzer.

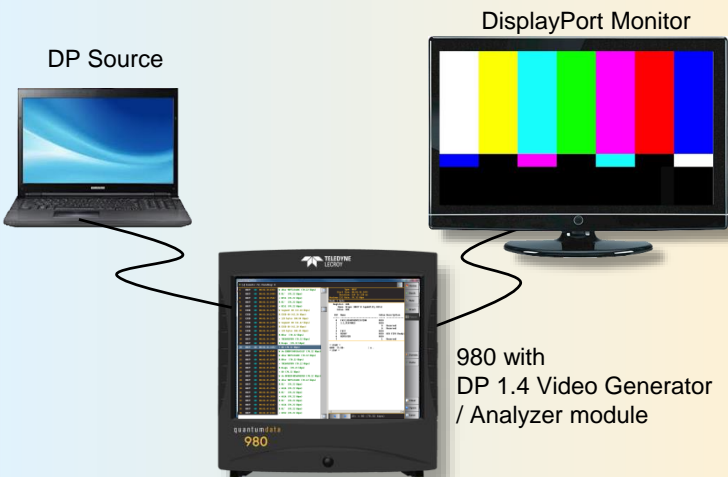
Capture and Decode (Filter View showing only Audio Packets)



DP Connection Sequence with DP Alt Mode Negotiations



Test Setup for Source Analysis (Capture/Decode)



Test Setup for Passive Aux Channel Monitoring

(Passive) Auxiliary Channel Analyzer

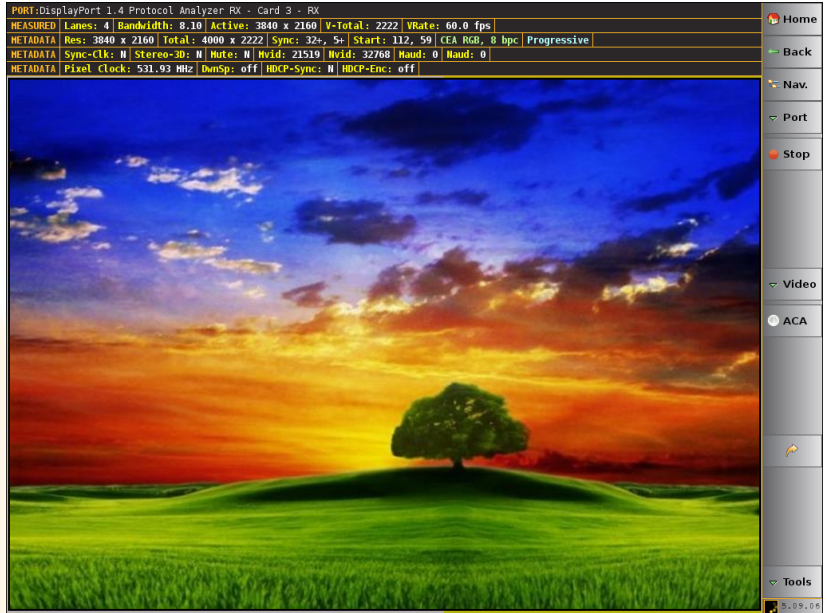
The 980 DP 1.4 Video Generator / Analyzer module's Adjunct Auxiliary Channel Analyzer board enables you to monitor the DP Aux Channel for link training and MST negotiations, HDCP transactions and EDID exchanges between a DisplayPort source and display device. This enables developers to investigate interoperability problems between DisplayPort devices involving link training, HDCP and EDID. Solution is provided using a custom cable provided by Teledyne LeCroy. The ACA logs these events and assigns precise timestamps to them. You can view the details of each transaction. These ACA logs can be saved and disseminated for further analysis by colleagues and other subject matter experts.

UPDATE! SOURCE ANALYSIS & AUX CHANNEL ANALYSIS

Analyzer

The 980 DP 1.4 module's Analyzer enables you to view the incoming video, link rate, timing, colorimetry and various other metadata at a glance. The Analyzer provides a basic confidence test to verify that the incoming video is essentially correct. The Rx port emulates any EDID to test a source devices handling of various EDIDs. You can also configure DPCD registers for emulating on the DP Rx port using the DPCD Editor (below).

Real Time Analysis



Admin Display for ATP Manager

DP HBR3-Capable Source device under test

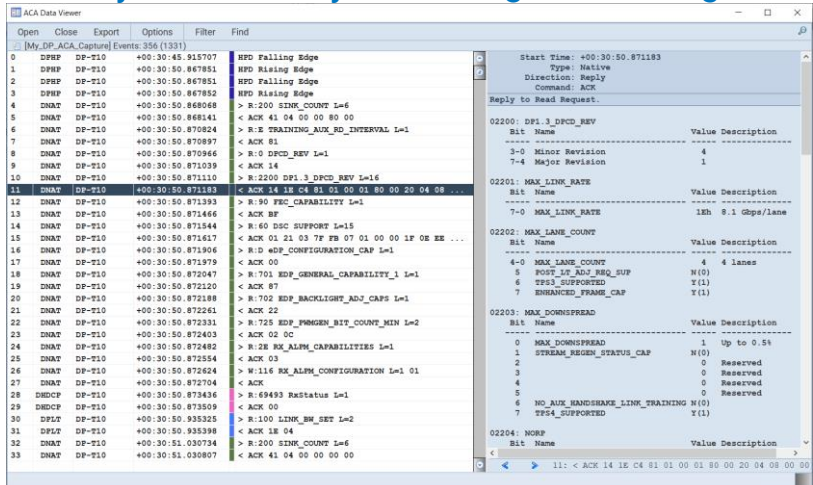
M41d

Source Test Setup

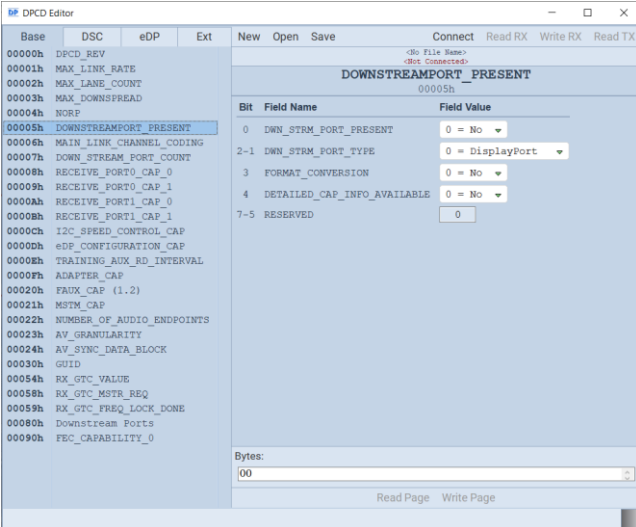
Aux Channel Analyzer (ACA)

The 980 DP 1.4 module's Auxiliary Channel Analyzer (ACA) feature enables you to monitor the DP Aux Channel for link training, MST negotiations, HDCP transactions and EDID exchanges between the M41d Rx port and a source device. The ACA logs the events and assigns precise timestamps to them. You can view the details of each transaction. These ACA logs can be saved and disseminated for further analysis by colleagues and other subject matter experts.

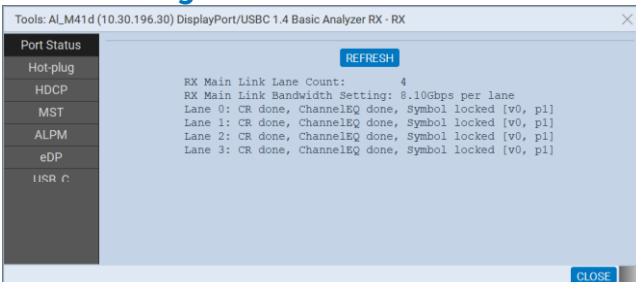
Auxiliary Channel Analyzer Showing Link Training



DPCD Editor

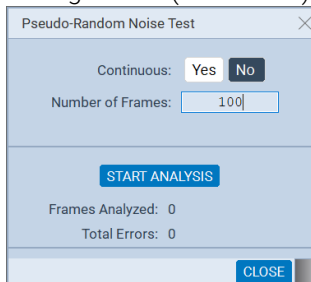


Link Training Status



Pixel Error Test for Cables and Distribution Devices

The M41d support a Pixel Error test (or a Pseudo-Random Noise tests for verifying cables and distribution equipment, The test is run in a loopback configuration (not shown).



DISPLAY STREAM COMPRESSION (DSC) TESTING

DSC Analysis

The 980 DP 1.4 Video Generator / Analyzer module's DSC analysis feature enables developers to view the DisplayPort DSC related protocol elements such as the picture parameter set, end of chunk packets and compression flag settings in the VBI to ensure that these elements are occurring in the video stream and that they are occurring in the proper sequence. The DSC analysis feature also captures and decompresses the video frames enabling developers to examine them for compression artifacts. The Forward Error Correction (FEC) transport mechanism, which ensures reliable, error free video transport, can also be verified.

DSC Analysis showing Picture Parameter Set (PPS)

The screenshot shows the DP Capture Viewer interface. The main window displays a timeline of data packets. A detailed view of a Picture Parameter Set (PPS) is shown on the right, including fields such as Packet ID, dsc_version_major, dsc_version_minor, pps_identifier, bits_per_component, linebuf_depth, block_jit_enable, convert_rgb, simple_422, vdr_enable, native_422, and Lane 3: 00 00 03 c0 c3 c0 aa 00 0f 00 0f. The interface also includes a search bar and various navigation controls.



980 DP 1.4 Video Generator / Analyzer module

Test Setup for Source Analysis (Capture/Decode)

ACA DPCD Reads for DSC Capabilities

The 980 DP 1.4 Video Generator / Analyzer module's ACA utility provides a log of the Aux Channel transactions. The link training can be viewed as well as the DPCD register reads and writes involved in the setup and maintenance of Display Stream Compression (DSC) and Forward Error Correction (FEC).

ACA showing DPCD reads for DSC capabilities

The screenshot shows the ACA Data Viewer interface. The main window displays a log of DPCD reads for DSC capabilities. A detailed view of the DSC SUPPORT register is shown on the right, including fields such as Bit Name, Value, and Description. The interface also includes a search bar and various navigation controls.

Video Generation (DSC/FEC)

The module's DSC/FEC video generator feature enables display developers to transmit DSC/FEC streams. Users can selection from several test patterns and configure the colorimetry, bits per component, bits per pixel, line buffer bit depth and DSC slice configurations.

DSC / FEC Video Generation

The screenshot shows the Generator interface. The main window displays the DSC Settings, including fields such as Color Mode, Slice Width (pixels), Slice Height (pixels), Line Buffer Bit Depth, and Bits Per Component. The interface also includes a search bar and various navigation controls.

980 with DisplayPort Video Generator / Analyzer

DisplayPort Monitor



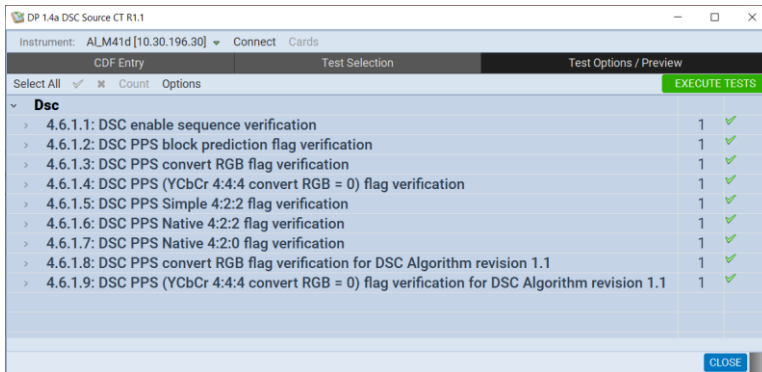
Test Setup for Sink Test

DISPLAY STREAM COMPRESSION (DSC) COMPLIANCE

DSC Compliance

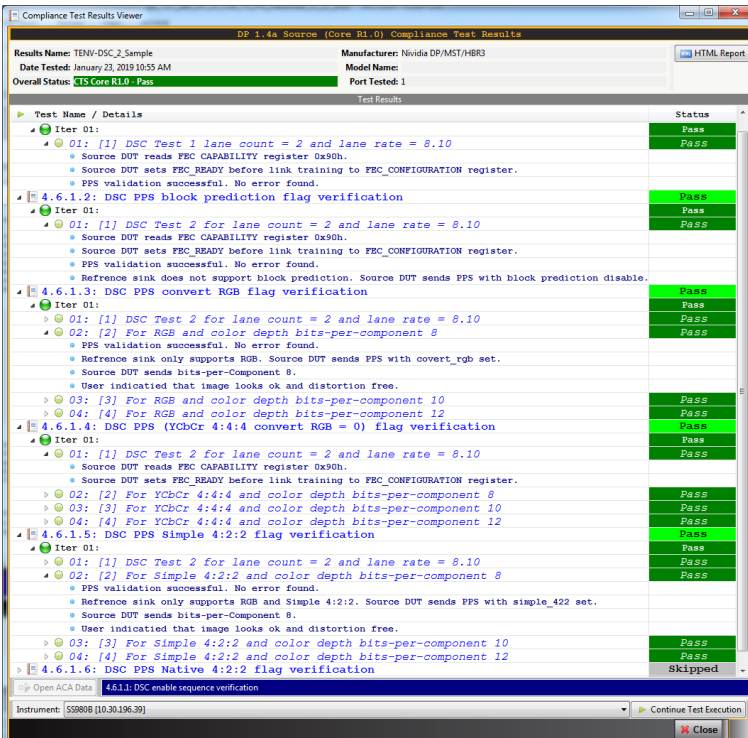
The 980 DSC source and sink compliance tests are ideal for pre-testing your DisplayPort source, sink or repeater product prior to submission to an Authorized Test Center for approval. Pre-testing provides assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the auxiliary channel analyzer traces logged during the test to help diagnose the cause of compliance test failures. (Refer to the test setups on the previous page.)

DSC Source Tests



Select All	#	Count	Options	Test Selection	Test Options / Preview
Dsc					
>	4.6.1.1:	DSC enable sequence verification	1	✓	
>	4.6.1.2:	DSC PPS block prediction flag verification	1	✓	
>	4.6.1.3:	DSC PPS convert RGB flag verification	1	✓	
>	4.6.1.4:	DSC PPS (YCbCr 4:4:4 convert RGB = 0) flag verification	1	✓	
>	4.6.1.5:	DSC PPS Simple 4:2:2 flag verification	1	✓	
>	4.6.1.6:	DSC PPS Native 4:2:2 flag verification	1	✓	
>	4.6.1.7:	DSC PPS Native 4:2:0 flag verification	1	✓	
>	4.6.1.8:	DSC PPS convert RGB flag verification for DSC Algorithm revision 1.1	1	✓	
>	4.6.1.9:	DSC PPS (YCbCr 4:4:4 convert RGB = 0) flag verification for DSC Algorithm revision 1.1	1	✓	

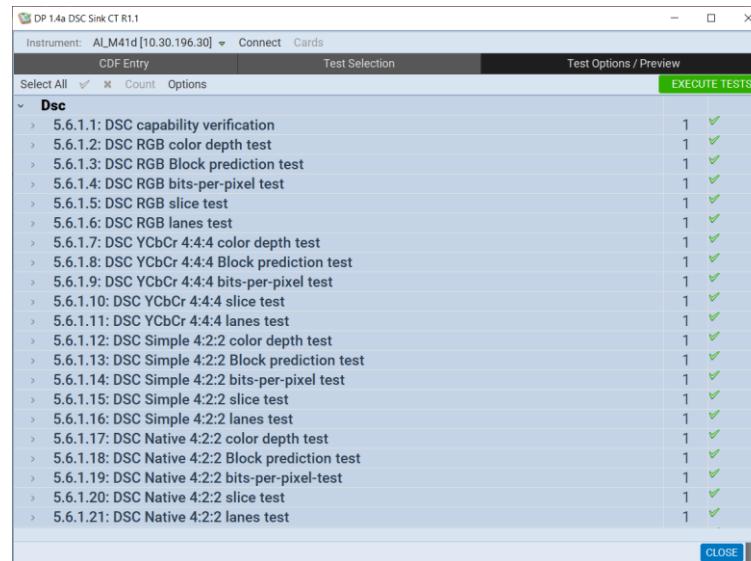
DSC Source Tests - Test Results



Results Name: TENV-DSC_2_Simple
Date Tested: January 21, 2019 5:14 AM
Overall Status: **CTS Core R1.0 - Pass**
Manufacturer: Nvidia DP/MSI/HBR3
Model Name:
Port Tested: 1

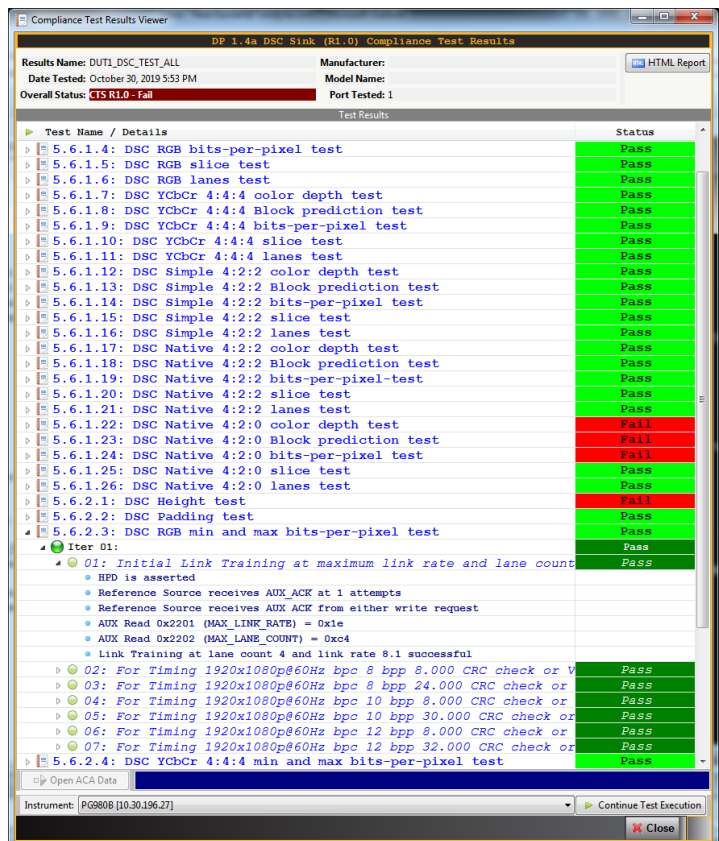
Test Name / Details	Status
Iter 01:	Pass
01: [1] DSC Test 1 lane count = 2 and lane rate = 8.10	Pass
02: [2] For RGB and color depth bits-per-component 8	Pass
03: [3] For YCbCr 4:4:4 and color depth bits-per-component 10	Pass
04: [4] For YCbCr 4:4:4 and color depth bits-per-component 12	Pass
4.6.1.2: DSC PPS block prediction flag verification	Pass
Iter 01:	Pass
01: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10	Pass
02: [2] For RGB and color depth bits-per-component 8	Pass
03: [3] For YCbCr 4:4:4 and color depth bits-per-component 10	Pass
04: [4] For YCbCr 4:4:4 and color depth bits-per-component 12	Pass
4.6.1.3: DSC PPS convert RGB flag verification	Pass
Iter 01:	Pass
01: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10	Pass
02: [2] For Simple 4:2:2 and color depth bits-per-component 8	Pass
03: [3] For Simple 4:2:2 and color depth bits-per-component 10	Pass
04: [4] For Simple 4:2:2 and color depth bits-per-component 12	Pass
4.6.1.4: DSC PPS (YCbCr 4:4:4 convert RGB = 0) flag verification	Pass
Iter 01:	Pass
01: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10	Pass
02: [2] For Simple 4:2:2 and color depth bits-per-component 8	Pass
03: [3] For Simple 4:2:2 and color depth bits-per-component 10	Pass
04: [4] For Simple 4:2:2 and color depth bits-per-component 12	Pass
4.6.1.5: DSC PPS Simple 4:2:2 flag verification	Pass
Iter 01:	Pass
01: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10	Pass
02: [2] For Simple 4:2:2 and color depth bits-per-component 8	Pass
03: [3] For Simple 4:2:2 and color depth bits-per-component 10	Pass
04: [4] For Simple 4:2:2 and color depth bits-per-component 12	Pass
4.6.1.6: DSC PPS Native 4:2:2 flag verification	Skipped

DSC Sink Tests



Select All	#	Count	Options	Test Selection	Test Options / Preview
Dsc					
>	5.6.1.1:	DSC capability verification	1	✓	
>	5.6.1.2:	DSC RGB color depth test	1	✓	
>	5.6.1.3:	DSC RGB Block prediction test	1	✓	
>	5.6.1.4:	DSC RGB bits-per-pixel test	1	✓	
>	5.6.1.5:	DSC RGB slice test	1	✓	
>	5.6.1.6:	DSC RGB lanes test	1	✓	
>	5.6.1.7:	DSC YCbCr 4:4:4 color depth test	1	✓	
>	5.6.1.8:	DSC YCbCr 4:4:4 Block prediction test	1	✓	
>	5.6.1.9:	DSC YCbCr 4:4:4 bits-per-pixel test	1	✓	
>	5.6.1.10:	DSC YCbCr 4:4:4 slice test	1	✓	
>	5.6.1.11:	DSC YCbCr 4:4:4 lanes test	1	✓	
>	5.6.1.12:	DSC Simple 4:2:2 color depth test	1	✓	
>	5.6.1.13:	DSC Simple 4:2:2 Block prediction test	1	✓	
>	5.6.1.14:	DSC Simple 4:2:2 bits-per-pixel test	1	✓	
>	5.6.1.15:	DSC Simple 4:2:2 slice test	1	✓	
>	5.6.1.16:	DSC Simple 4:2:2 lanes test	1	✓	
>	5.6.1.17:	DSC Native 4:2:2 color depth test	1	✓	
>	5.6.1.18:	DSC Native 4:2:2 Block prediction test	1	✓	
>	5.6.1.19:	DSC Native 4:2:2 bits-per-pixel-test	1	✓	
>	5.6.1.20:	DSC Native 4:2:2 slice test	1	✓	
>	5.6.1.21:	DSC Native 4:2:2 lanes test	1	✓	

DSC Sink Tests - Test Results



Results Name: DUT1_DSC_TEST_ALL
Date Tested: October 30, 2019 5:33 PM
Overall Status: **CTS R1.0 - Fail**
Manufacturer:
Model Name:
Port Tested: 1

Test Name / Details	Status
5.6.1.4: DSC RGB bits-per-pixel test	Pass
5.6.1.5: DSC RGB slice test	Pass
5.6.1.6: DSC RGB lanes test	Pass
5.6.1.7: DSC YCbCr 4:4:4 color depth test	Pass
5.6.1.8: DSC YCbCr 4:4:4 Block prediction test	Pass
5.6.1.9: DSC YCbCr 4:4:4 bits-per-pixel test	Pass
5.6.1.10: DSC YCbCr 4:4:4 slice test	Pass
5.6.1.11: DSC YCbCr 4:4:4 lanes test	Pass
5.6.1.12: DSC Simple 4:2:2 color depth test	Pass
5.6.1.13: DSC Simple 4:2:2 Block prediction test	Pass
5.6.1.14: DSC Simple 4:2:2 bits-per-pixel test	Pass
5.6.1.15: DSC Simple 4:2:2 slice test	Pass
5.6.1.16: DSC Simple 4:2:2 lanes test	Pass
5.6.1.17: DSC Native 4:2:2 color depth test	Pass
5.6.1.18: DSC Native 4:2:2 Block prediction test	Pass
5.6.1.19: DSC Native 4:2:2 bits-per-pixel-test	Pass
5.6.1.20: DSC Native 4:2:2 slice test	Pass
5.6.1.21: DSC Native 4:2:2 lanes test	Pass
5.6.1.22: DSC Native 4:2:0 color depth test	Fail
5.6.1.23: DSC Native 4:2:0 Block prediction test	Fail
5.6.1.24: DSC Native 4:2:0 bits-per-pixel test	Fail
5.6.1.25: DSC Native 4:2:0 slice test	Pass
5.6.1.26: DSC Native 4:2:0 lanes test	Pass
5.6.2.1: DSC Height test	Fail
5.6.2.2: DSC Padding test	Pass
5.6.2.3: DSC RGB min and max bits-per-pixel test	Pass
Iter 01:	Pass
01: Initial Link Training at maximum link rate and lane count	Pass
02: For Timing 1920x1080p@60Hz bpc 8 bpp 8.000 CRC check or V	Pass
03: For Timing 1920x1080p@60Hz bpc 8 bpp 24.000 CRC check or	Pass
04: For Timing 1920x1080p@60Hz bpc 10 bpp 8.000 CRC check or	Pass
05: For Timing 1920x1080p@60Hz bpc 10 bpp 30.000 CRC check or	Pass
06: For Timing 1920x1080p@60Hz bpc 12 bpp 8.000 CRC check or	Pass
07: For Timing 1920x1080p@60Hz bpc 12 bpp 32.000 CRC check or	Pass
5.6.2.4: DSC YCbCr 4:4:4 min and max bits-per-pixel test	Pass

DP 1.4 LINK LAYER SOURCE COMPLIANCE

Source Link Layer Compliance **Approved!**

The 980 DP source HBR3 link layer compliance tests are approved by VESA and are ideal for self-testing or pre-testing your HBR3-capable DisplayPort 1.4 source product prior to submission to an Authorized Test Center for approval. Pre-testing provides added assurance that your product will pass at the ATC when submitted. The compliance tests (below right) enable you to view the captured data and detailed test results which help pinpoint the cause of compliance test failures. The link layer compliance test suite now includes tests for forward error correction (FEC). You can link to the aux channel traces in the Aux Channel Analyzer (ACA) to view the root cause of failures (below).

DP 1.4 Source Link Layer Compliance - Test Selection

Test Item	Status
AUX Rtd. after HPD	
4.2.1.1: Source DUT Retry on No-Reply During AUX Read after HPD Plug Event	1 ✓
4.2.1.2: Source Retry on Invalid Reply During AUX Read after HPD Plug Event	1 ✓
4.2.1.3: Source Device HPD Event Pulse Length Test	1 ✓
4.2.1.4: Source Device IRQ_HPDP Pulse Length Test	1 ✓
4.2.1.5: Source Device Inactive HPD / Inactive AUX Test	1 ✓
EDID and DPCD Rtd.	
4.2.2.1: DPCD Receiver Capability and EDID Read upon HPD Plug Event	1 ✓
4.2.2.2: DPCD Extended Receiver Capability and EDID Read upon HPD Plug Event	1 ✓
4.2.2.3: EDID Read	1 ✓
4.2.2.4: EDID Read Failure #1: I2C-Over-AUX NACK	1 ✓
4.2.2.5: EDID Read Failure #2: I2C-Over-AUX DEFER	1 ✓
4.2.2.6: EDID Corruption Detection	1 ✓
4.2.2.7: Branch Device Detection upon HPD Plug Event	1 ✓
4.2.2.8: EDID Read on IRQ_HPDP Event after Branch Device Detection	1 ✓
4.2.2.9: E-DDC Four Block EDID Read	1 ✓
4.2.2.10: Link Status/Adjust Request AUX read interval during Link Training	1 ✓
Link Training	
4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds	1 ✓
4.3.1.2: Successful Link Training Upon HPD Plug Event	1 ✓
4.3.1.3: Successful Link Training (Higher Differential Voltage Swing during Clock Recovery)	1 ✓
4.3.1.4: Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing	1 ✓
4.3.1.5: Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing	1 ✓

DP Source



980 DP 1.4 Video Generator / Analyzer module



Test Setup for Source Compliance (Capture/Decode)

DP 1.4 Source Link Layer Compliance Test

Results Name: 03_27_2018_15_33_45
 Date Tested: March 27, 2018 3:33 PM
 Overall Status: **CTS 1.4 Core R1.0 - Pass**

Test Name / Details	Status
4.3.2.1: Successful Link Re-training After IRQ_HPDP Pulse Due to Loss of Symbol	Pass
Iter 01:	Pass
01: [1] Link Maintenance test for lane count = 4 and lane rate = 8.10	Pass
02: [2] After Sym lock error on lane 1, Link Maintenance test for lane cou	Pass
03: [3] After Sym lock error on lane 2, Link Maintenance test for lane cou	Pass
04: [4] After Sym lock error on lane 3, Link Maintenance test for lane cou	Pass
05: [5] After Sym lock error on lane 4, Link Maintenance test for lane cou	Pass
4.3.2.2: Successful Link Re-training After IRQ_HPDP Pulse Due to Loss of Clock F	Pass
4.3.2.3: Successful Link Re-training After IRQ_HPDP Pulse Due to Loss of Inter-l	Pass
4.3.2.4: Handling of IRQ_HPDP Pulse with No Error Status Bits Set.	Pass
4.3.2.5: Lane Count Reduction and Increase.	Pass

DP Aux Channel Traces – From LLC Test

Time	Direction	Command
39	DP->R31	< ACK
40	DP->R31	> R:R TRAINING_AUX_RD_INTERVAL L=1
41	DP->R31	< ACK 81
42	DP->R31	> W:100 LINK_RM_SET L=1 06
43	DP->R31	< ACK
44	DP->R31	> W:101 LANE_COUNT_SET L=1 81
45	DP->R31	< ACK
46	DP->R31	> W:102 TRAINING_PATTERN_SET: L=1 21
47	DP->R31	< ACK
48	DP->R31	> W:103 TRAINING_LANE0_SET L=4 00 00 00 00
49	DP->R31	< ACK
50	DP->R31	> R:202 LANE_I_STATUS L=2
51	DP->R31	< DEFER
52	DP->R31	> R:202 LANE_I_STATUS L=2
53	DP->R31	< DEFER
54	DP->R31	> R:202 LANE_I_STATUS L=2
55	DP->R31	< DEFER
56	DP->R31	> R:202 LANE_I_STATUS L=2
57	DP->R31	< DEFER
58	DP->R31	> R:202 LANE_I_STATUS L=2
59	DP->R31	< DEFER
60	DP->R31	> R:202 LANE_I_STATUS L=2
61	DP->R31	< DEFER
62	DP->R31	> R:202 LANE_I_STATUS L=2
63	DP->R31	< ACK 01 00
64	DP->R31	> W:102 TRAINING_PATTERN_SET: L=1 07
65	DP->R31	< ACK
66	DP->R31	> W:103 TRAINING_LANE0_SET L=4 00 00 00 00
67	DP->R31	< ACK
68	DP->R31	> R:202 LANE_I_STATUS L=2
69	DP->R31	< ACK 01 00 00
70	DP->R31	> R:204 LANE_ALIGN_STATUS_UPDATED L=2
71	DP->R31	< ACK 00 03
72	DP->R31	> R:204 ADJUST_REQUEST_LANE0_1 L=2
73	DP->R31	< ACK 44 44

DP 1.4 LINK LAYER SINK COMPLIANCE

Sink Link Layer Compliance Approved!

The 980 DP sink (display) link layer compliance tests are ideal for pre-testing your DisplayPort 1.4 display product prior to submission to an Authorized Test Center for approval. Pre-testing provides added assurance that your product will pass at the ATC when submitted. The compliance tests (below right) enable you to view the captured data and detailed test results which help pinpoint the cause of compliance test failures. The link layer compliance test suite now includes tests for forward error correction (FEC). You can link to the aux channel traces in the Aux Channel Analyzer (ACA) to view the root cause of failures (below).

980 with
DP 1.4 Video Generator
/ Analyzer module



DisplayPort Monitor



Test Setup for Sink Test

DP 1.4 Link Layer Compliance - Test Selection

Test Name	Count	Options	Status
5.2.1.1: Read One Byte from Valid DPCD Address	1		Pass
5.2.1.2: DPCD Receiver Capability Read (Read 12 Bytes from Valid DPCD Address)	1		Pass
5.2.1.3: Write One Byte to Valid DPCD Address	1		Pass
5.2.1.4: Write Nine Bytes to Valid DPCD Addresses	1		Pass
5.2.1.5: Write EDID Offset (One Byte I2C-Over-AUX Write)	1		Pass
5.2.1.6: Read One EDID Byte (One Byte I2C-Over-AUX Read)	1		Pass
5.2.1.7: EDID Read	1		Pass
5.2.1.8: Illegal AUX Request Syntax	1		Pass
5.2.1.9: Glitch Rejection	1		Pass
5.2.1.10: Interleaved EDID and DPCD Receiver Capability Read	1		Pass
5.2.1.11: Downstream Stop on MOT Reset	1		Pass
5.2.1.12: Downstream Stop on Timeout	1		Pass
5.2.2.1: Sink Organizationally Unique Identifier (OUI)	1		Pass
5.2.2.2: Sink Count	1		Pass
5.2.2.3: Sink Status	1		Pass
5.2.2.4: Sink Error Count	1		Pass
5.2.2.5: DPCD Address Range	1		Pass
5.2.2.6: Number of Receiver Ports	1		Pass
5.2.2.7: Main Link Channel Coding	1		Pass
5.2.2.8: ESI Field Mapping	1		Pass

DP 1.4 Link Layer Compliance - Test Results

Test Name / Details	Status
5.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds	Pass
Iter 01:	Pass
01: Link Training test for lane count = 1 and lane rate = 1.62	Pass
02: Link Training test for lane count = 2 and lane rate = 1.62	Pass
03: Link Training test for lane count = 4 and lane rate = 1.62	Pass
04: Link Training test for lane count = 1 and lane rate = 2.70	Pass
05: Link Training test for lane count = 2 and lane rate = 2.70	Pass
06: Link Training test for lane count = 4 and lane rate = 2.70	Pass
07: Link Training test for lane count = 1 and lane rate = 5.40	Pass
08: Link Training test for lane count = 2 and lane rate = 5.40	Pass
09: Link Training test for lane count = 4 and lane rate = 5.40	Pass
10: Link Training test for lane count = 1 and lane rate = 8.10	Pass
11: Link Training test for lane count = 2 and lane rate = 8.10	Pass
12: Link Training test for lane count = 4 and lane rate = 8.10	Pass
5.3.1.2: Successful Link Training with Request of Higher Differential Voltage	Pass
5.3.1.3: Successful Link Training to a Lower Link Rate Due to Clock Recovery L	Pass
5.3.1.4: Successful Link Training with Request of a Change to Pre-Emphasis and	Pass
Iter 01:	Pass
01: Link Training test for lane count = 4 and lane rate = 8.10	Pass

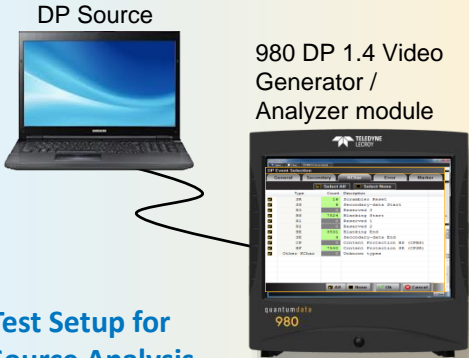
DP Aux Channel Traces – From LLC Test

Time	Channel	Event	Description
00:30:45.915707	DP-210	RFD Falling Edge	
00:30:45.915707	DP-210	RFD Rising Edge	
00:30:45.915707	DP-210	RFD Falling Edge	
00:30:45.915707	DP-210	RFD Rising Edge	
00:30:45.915707	DP-210	R:200 SINK_COUNT L=4	
00:30:45.915707	DP-210	< ACK 41 04 00 00 00 00	
00:30:45.915707	DP-210	R:8E TRAINING_AUX_ID_INTERVAL L=1	
00:30:45.915707	DP-210	< ACK 81	
00:30:45.915707	DP-210	R:0 DPCD_REV L=1	
00:30:45.915707	DP-210	< ACK 14	
00:30:45.915707	DP-210	R:2200 DP1_3_DPCD_REV L=16	
00:30:45.915707	DP-210	< ACK 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	
00:30:45.915707	DP-210	R:30 RFD_CAPABILITY L=1	
00:30:45.915707	DP-210	< ACK 8F	
00:30:45.915707	DP-210	R:60 RFD_SUPPORT L=1	
00:30:45.915707	DP-210	< ACK 01 21 03 7F 07 01 00 00 0F 0E 0E ...	
00:30:45.915707	DP-210	R:10 MDP_CONFIGURATION_CAP L=1	
00:30:45.915707	DP-210	< ACK 05	
00:30:45.915707	DP-210	R:701 RFD_GENERAL_CAPABILITY_1 L=1	
00:30:45.915707	DP-210	< ACK 87	
00:30:45.915707	DP-210	R:702 RFD_BACKLIGHT_ADJ_CAPS L=1	
00:30:45.915707	DP-210	< ACK 22	
00:30:45.915707	DP-210	R:725 RFD_FPMEN_BIT_COUNT_MIN L=2	
00:30:45.915707	DP-210	< ACK 02 0C	
00:30:45.915707	DP-210	R:18 RFD_RX_ALPM_CAPABILITIES L=1	
00:30:45.915707	DP-210	< ACK 03	
00:30:45.915707	DP-210	R:116 RX_ALPM_CONFIGURATION L=1 01	
00:30:45.915707	DP-210	< ACK 4	
00:30:45.915707	DP-210	R:69493 Rstatus L=1	
00:30:45.915707	DP-210	< ACK 00	
00:30:45.915707	DP-210	R:0 LINK_RATE_SET L=2	
00:30:45.915707	DP-210	< ACK 18 04	
00:30:45.915707	DP-210	R:200 SINK_COUNT L=4	
00:30:45.915707	DP-210	< ACK 41 04 00 00 00 00	

HDCP 2.2 SOURCE, SINK & REPEATER COMPLIANCE

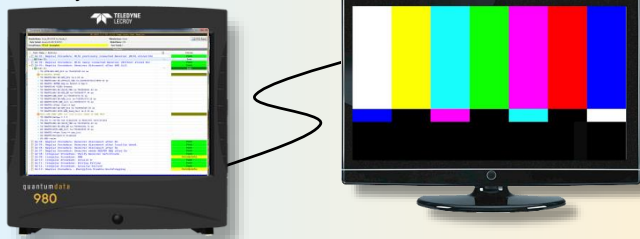
HDCP 2.2 Compliance

The 980 HDCP 2.2 compliance tests are ideal for pre-testing your DisplayPort source, sink or repeater product prior to submission to an Authorized Test Center for approval. Pre-testing provides assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the auxiliary channel analyzer traces logged (not shown) during the test to help diagnose the cause of compliance test failures.



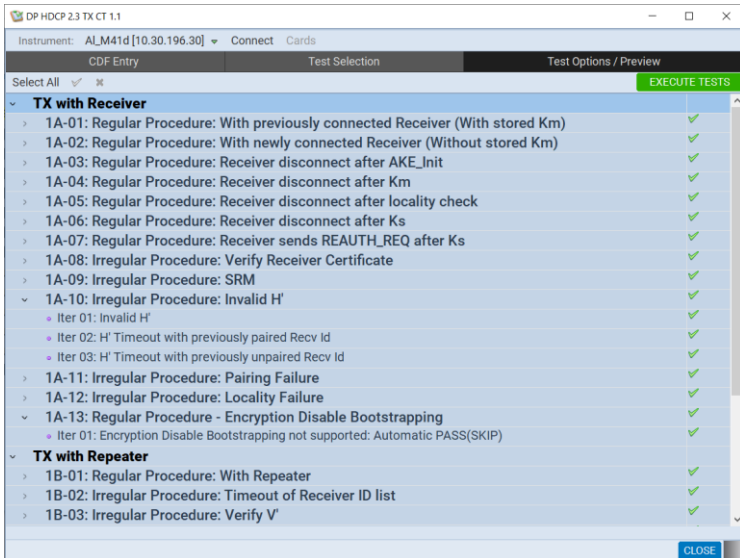
Test Setup for Source Analysis (Capture/Decode)

980 with DP 1.4 Video Generator / Analyzer module

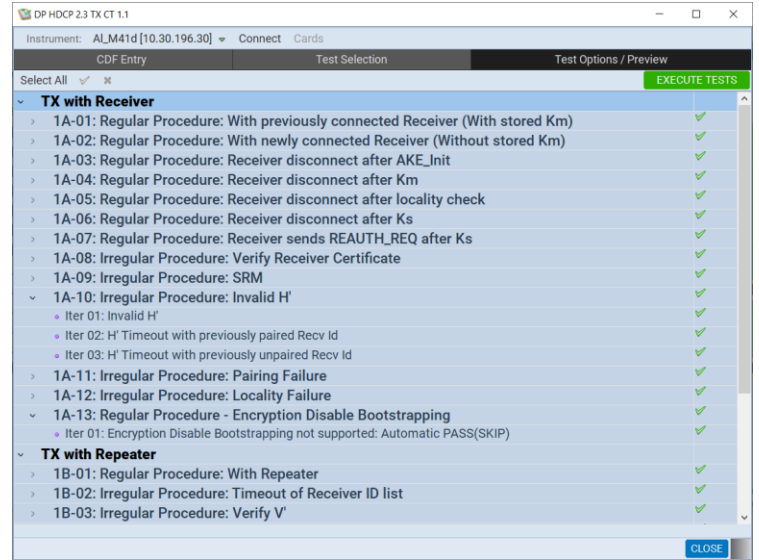


Test Setup for Sink Test

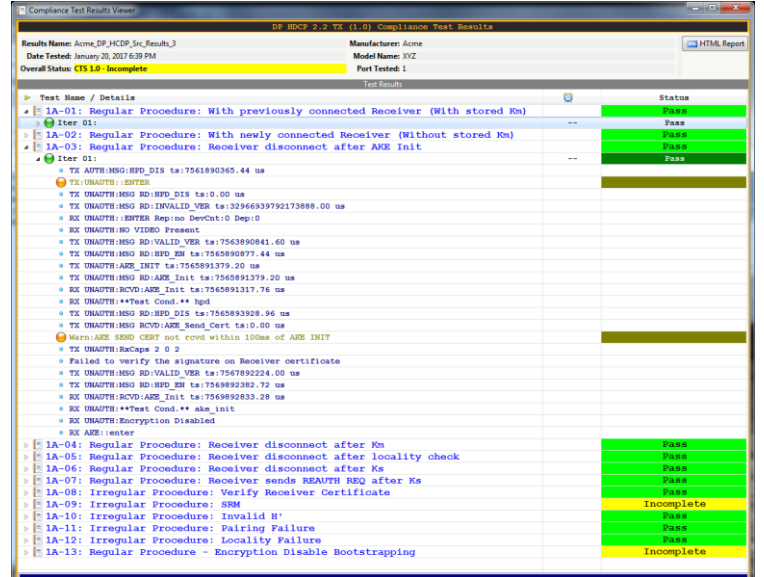
HDCP 2.2 Sink Tests - Test Selection



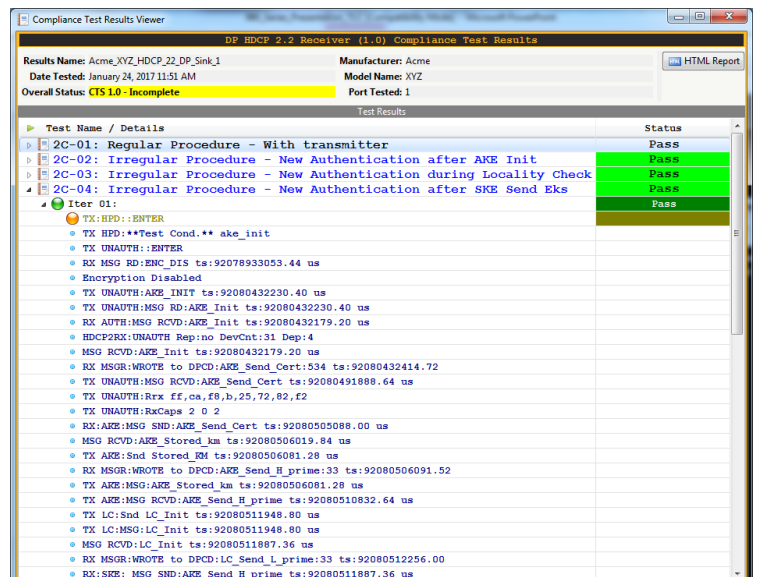
HDCP 2.2 Source Tests - Test Selection



HDCP 2.2 Source Tests - Test Results



HDCP 2.2 Sink Tests - Test Results

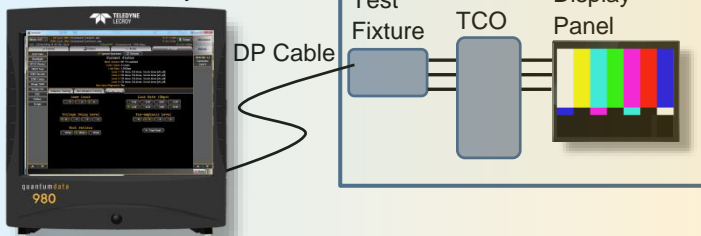


EMBEDDED DISPLAYPORT (EDP) 1.4B TESTING

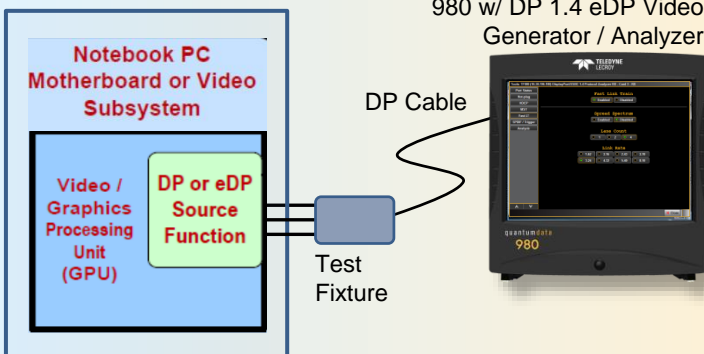
Embedded DisplayPort eDP - ALPM

The 980 DP 1.4 USB-C/eDP Video Generator / Analyzer supports testing of both eDP source and display subsystems. A standard DP connection from the 980 DP 1.4 eDP-capable module to a test fixture is required to enable connection to the eDP subsystem. For display panel TCON testing, once the connection is made, you can use the Advanced Link Power Management (ALPM) feature to test the display's ALPM function (right) and run any other video tests using the DP 1.4 module's Video Generation function. For eDP source subsystem testing, you can monitor the link training and ALPM state and run captures for analysis, etc. The test setups are shown below.

980 w/ DP 1.4 eDP Video Generator / Analyzer



Test Setup for eDP TCON Display Subsystem



Test Setup for testing eDP source Subsystem

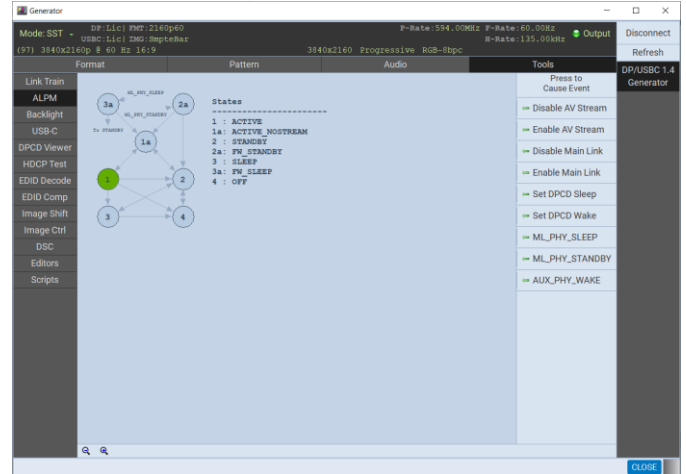
eDP Fast Link Training

The 980 DP 1.4 USB-C/eDP Video Generator / Analyzer supports fast link training acting either as an eDP source subsystem or an eDP display subsystem. The module emulates the necessary Fast Link training DPCD registers. When testing a display you can select the Lane Count, Link rate (including "intermediate" eDP lane rates), Voltage Swing, Pre-Emphasis and Training Test Pattern. You can monitor the Aux Channel transactions with the 980 Aux Channel Analyzer utility. (eDP Fast Link Training Source test not shown.)

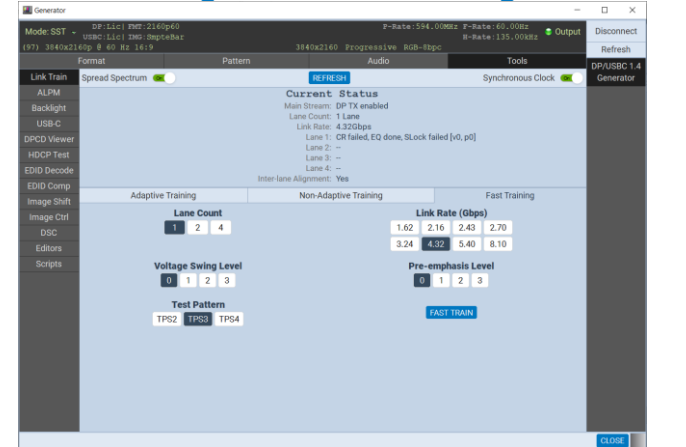
eDP Tx Backlight Control

The 980 DP 1.4 USB-C/eDP module supports testing of the eDP backlight control function on eDP TCON display subsystems. Backlight control is supported through the Aux Channel and the backlight control lead. The connection is made through the module's eDP header pins on the faceplate. You can select between High and Low backlight enable, set the PWM duty cycle, pre-scaling and PWM generator divider.

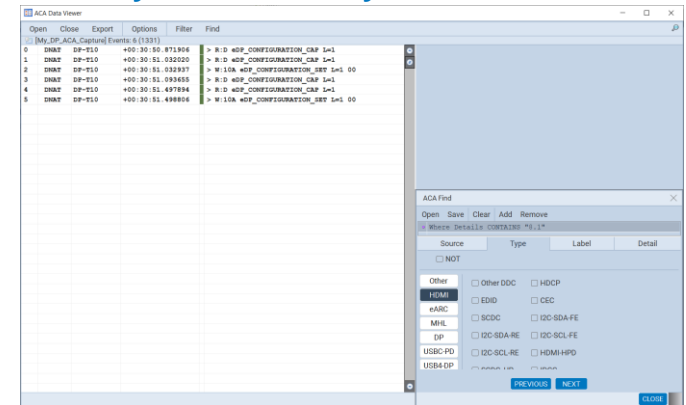
Advanced Link Power Management (ALPM)



Link Training Control and Configuration



Auxiliary Channel Analyzer – Fast Link Train



eDP Tx Backlight Control



SPECIFICATIONS

DisplayPort 1.4 / USB-C/ eDP Module

Version	DisplayPort 1.4a
Standard Formats	VESA, CTA
Connectors/Ports	
DP Full-Size	Tx (1) DP Full-size; Rx (1) DP Full-size
USB-C	Tx (1) USB-C with DP Alt Mode; Rx (1) USB-C with DP Alt Mode
eDP Header	Pins to access eDP Tx backlight controls
Aux Chan Adjunct Board	Tx (1), DP Full-size; Rx (1) DP Full-size
Protocol	DisplayPort
Video Data Rates	1.62, 2.7, 5.4, 8.1 Gb/s Link rates 1, 2, 4 Lanes
Color Depths	8, 10, 12, 16 bits
Video Encoding	RGB, YCbCr
Video Sampling Modes	4:4:4, 4:2:2, 4:2:0
HDCP	Versions 2.2 & (1.3 on 1 & 2 lanes only)
Audio	8 Channel LPCM programmable sine wave
Capture memory	8 GBytes

Options

DisplayPort Tx / Rx	Either or both: - DP Tx for display testing; selectable between DP Standard and USB-C - DP Rx port, two options; selectable between DP Standard and USB-C: - Basic Analyzer - Capture/Store Protocol Analyzer (requires Basic analyzer option)
DP Passive Aux Channel Analyzer	Monitor DisplayPort Aux Channel transactions in real time passively between a source or sink. Includes custom cable and Aux Adjunct board.
DP Capture Analysis of DSC Streams	Capture and analyze incoming Display Stream Compression (DSC) streams. There are no limits on the number of DSC slices for analysis.
DP Video Generation of DSC/FEC Streams	Select from a variety of DSC/FEC test patterns. Select colorimetry and configure slices. There are no limits on the number of DSC slices supported.
DP HDCP 2.2 Compliance Test	Run HDCP 2.2 compliance test on DisplayPort sources, sinks and repeaters (3 separate options) – Now Approved by DCP.
DP 1.4 Source Link Layer Compliance (Package #3)	Run DisplayPort 1.4 source Link Layer compliance test. (Sections: 4.3.1, 4.3.2, 4.3.3, 4.4.4, 4.5.1 [FEC])
DP 1.4 Sink Link Layer Compliance (Package #4)	Run DisplayPort 1.4 sink Link Layer compliance test (displays). (Sections: 5.2.1, 5.3.1, 5.3.2, 5.4.1/2 5.4.3, 5.4.4, 5.5.1 [FEC].)
DP 1.4 Sink EDID Compliance.	Run DisplayPort 1.4 sink EDID/DisplayID compliance test (displays).
NEW! DP 1.4 Source EDID Comp.	Run DisplayPort 1.4 source EDID/DisplayID compliance test.
DP 1.4 Source DSC/FEC Compliance	Run DisplayPort 1.4 source DSC/FEC compliance test Sections. 4.6.1/4.5.1.1. Requires 64-bit 980 system.
DP 1.4 Sink DSC/FEC Compliance	Run DisplayPort 1.4 Sink DSC/FEC compliance test. Sections 5.6.1, 5.6.2/5.5.1.1
Embedded DisplayPort (eDP) 1.4b	Test eDP source and display devices using fast link training, Advanced Link Power Management (ALPM) and backlight control testing of displays.

980 Test Platforms

Embedded Display	980B: 15" diagonal; Resolution: 1024(H); x 768 (V) resolution; 24 bit RGB color. 980R: 7" diagonal; Resolution: 800 (H) x 480 (V); 24 bit RGB color.
Power	90-264 VAC, 47-63Hz
Weight	23.76 LBS; 10.78 Kg
Size	980B: Height: 15.25 in. (38.7cm) Width: 14.57in. (36.5cm) Depth: 6.29in. (15.9cm) 980R: Height: 6.29 in. (15.9cm); Width: 15.25in. (38.7cm); Depth: 14.57in. (36.5cm)
Command Line Control	Ethernet (RJ-45) for external GUI and telnet
Environmental	Operating Temp: 32 to 104 (F); 0 to 40 (C)



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