

quantumdata™ 980 48G Protocol Analyzer / Generator module

for HDMI® Testing
Deep Analysis & Generation of Fixed Rate Link (FRL)
with Forward Error Correction (FEC)
Now Supports Gaming Compliance Testing!



Key Features

- View incoming FRL and TMDS (encrypted or unencrypted) video frames and video metadata and timing in real time
- Use generator or analyzer in three (3) and four (4) lane configurations at all lane rates: 3Gbps, 6Gbps, 8Gbps, 10Gbps and 12Gbps (48Gbps aggregate)
- Video generator function supports TMDS and FRL for video resolutions up to 8K and 10K resolutions
- Certified “Test Device Approved for Dolby Labs, Inc.” for HDMI and eARC Dolby audio generation & analysis including Dolby Vision Source Led tests
- Evaluate 4K and 8K HDR10 UHD TVs with HDR Lab
- View captured FRL and TMDS data elements graphically in Event Plot and in Data Decode table; use searching and filtering to find data
- View FRL packet mapping into Character Blocks and Character Block mapping into Super Blocks
- Verify Display Stream Compression (DSC) on FRL, DSC capable sources or sinks
- Run FRL source & sink compliance tests
- Run DSC sink & source compliance tests
- View embedded TMDS video, protocol and metadata elements, in FRL stream
- Monitor of FRL Link Training transactions in the Auxiliary Channel Analyzer (ACA) utility to show SCDC reads and writes over the DDC channel
- Run pixel error test on incoming TMDS streams
- Passively monitor DDC channel in TMDS or FRL mode (FRL mode requires custom cable)
- Passively monitor TMDS video and metadata (without HDCP) and DDC between a source and sink (requires both Tx and Rx licenses)
- View Lane Error Counts and Reed Solomon Counts in the SCDC CED registers
- Verify the eARC common mode channel on either an eARC Tx or Rx device
- Run eARC compliance tests on an eARC Tx or Rx device; all tests supported
- Run HDCP 2.3 source compliance tests
- Run HDMI TMDS source and sink compliance tests
- **NEW!** Gaming-VRR and Fast VActive and QMS-VRR
- Run HDR10+ Source Side Tone Mapping tests on UHD TVs
- Tests Power Cable Assemblies (PCA) for power requests
- Run test automation for compliance tests with the API

The Teledyne LeCroy quantumdata 980 48G Protocol Analyzer / Generator module for HDMI Testing is equipped with HDMI Tx and Rx ports supporting HDMI 2.1a Fixed Rate Link and FEC capture analysis and decode up to 48Gbps (12Gbps/Lane). The HDMI Rx analyzer port provides visibility into the Fixed Rate Link packetization—super blocks, character blocks and FRL packets and underlying TMDS video, protocol, control and metadata elements. The HDMI Tx video generator port transmits Fixed Rate Link video streams with embedded TMDS video, protocol, control and metadata elements. Supports Display Stream Compression (DSC) for testing both sources and sinks (including compliance testing). Supports FRL source and sink compliance testing. The module also supports the link training functions of the source and sink functions in the FRL mode in both 3 and 4 lane configurations. Enhanced Audio Return Channel (eARC) compliance testing is also supported for eARC Tx and eARC Rx devices.

FRL Analysis & Generation eARC Testing

The 980 48G Protocol Analyzer / Generator module provides video generation and deep analysis test features necessary to test the development of your HDMI 2.1 TMDS and FRL-capable source and sink devices. These features enable developers to identify and resolve interoperability problems early in the product life cycle. The enhanced FRL generator enables transmission of FRL and TMDS video streams through the HDMI Tx port. Supports user-selection of resolution (including 8K), frame rates, colorimetry, chroma sampling and color space.

The 980 48G Protocol Analyzer / Generator module supports functional testing and compliance testing of enhanced Audio Return Channel sources Tx devices (e.g. UHD TV) and eARC Rx, devices e.g. sound bar).

Operation

The 980 48G Protocol Analyzer / Generator module supports video generation and analysis of the FRL/FEC HDMI data streams through the user friendly 980 Manager which presents the data in an easy to understand way.

FIXED RATE LINK (FRL) ANALYSIS

Capture and Decode (FRL & FEC)

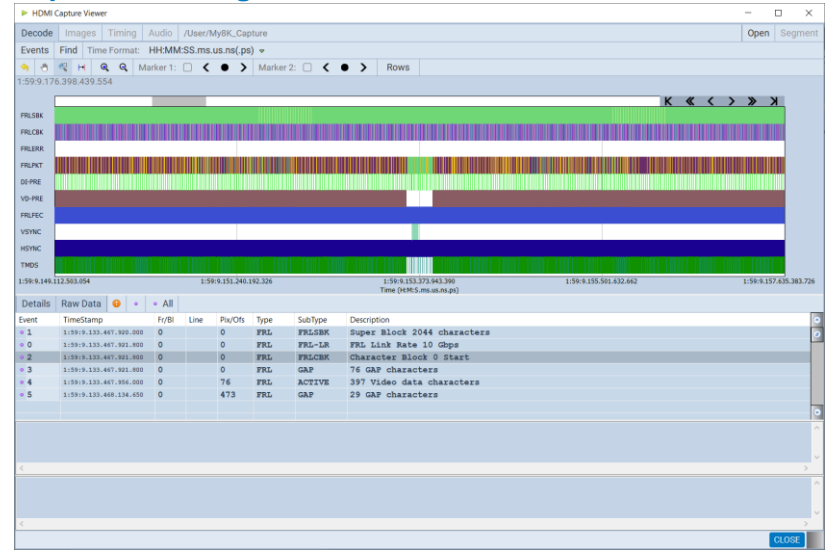
The 980 48G Protocol Analyzer / Generator module captures and decodes incoming HDMI® 2.1 streams (encrypted or unencrypted) that have been packetized with Fixed Rate Link packet structures. These FRL-related data elements are depicted graphically in the Event Plot . The decoded data and the raw data is shown in table form in the Data Decode window.

The Forward Error Correction (FEC) characters are also shown as appended on the Character Blocks. The module reports the Lane Error Counts and the FEC Reed Solomon Corrections Count in the SCDC CED registers.

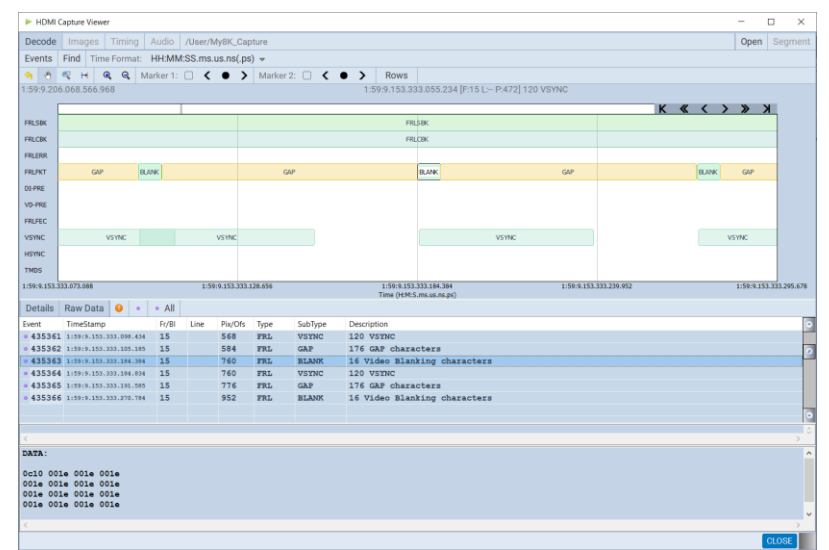
The underlying TMDS video and protocol elements such as the active video, data island and preamble blocks, are also depicted and decoded.

Each element is assigned a precise time stamp. Users can search and filter the FRL captured data by type.

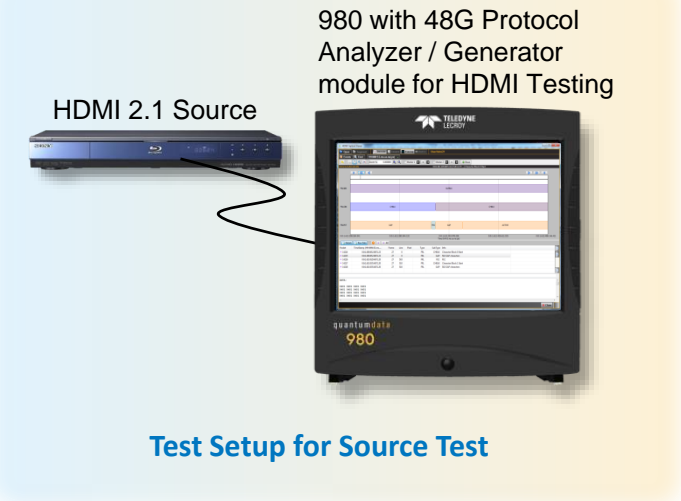
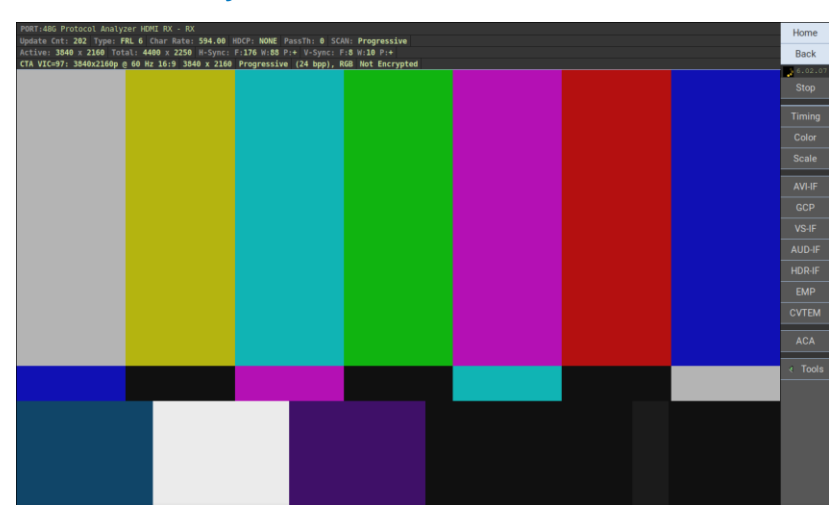
Capture Showing SCDC, FRL & TMDS Elements



Capture with FRL Elements & TMDS Video & Data Islands



Real Time Analysis



Test Setup for Source Test

Real Time Analysis

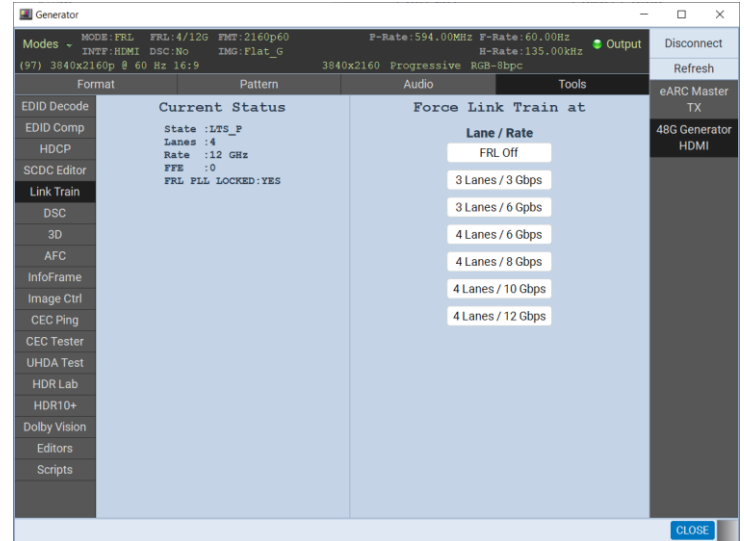
The module's Real Time analysis feature enables you to monitor the incoming TMDS and FRL video and metadata, data islands and InfoFrames including High Dynamic Range (HDR) InfoFrames. A status bar at the top of the window provides an at-a-glance view of the essential incoming video parameters.

FIXED RATE LINK (FRL) LINK TRAINING ANALYSIS

Link Training

The 980 48G Protocol Analyzer / Generator module supports Link Training configuration. The module emulates an HDMI 2.1 sink indicating the max FRL rate in the HF-VSDB of the EDID and various other essential link training parameters in the SCDC control registers.

Link Training Status Screen



980 with 48G Protocol Analyzer / Generator module for HDMI Testing

HDMI 2.1 Source

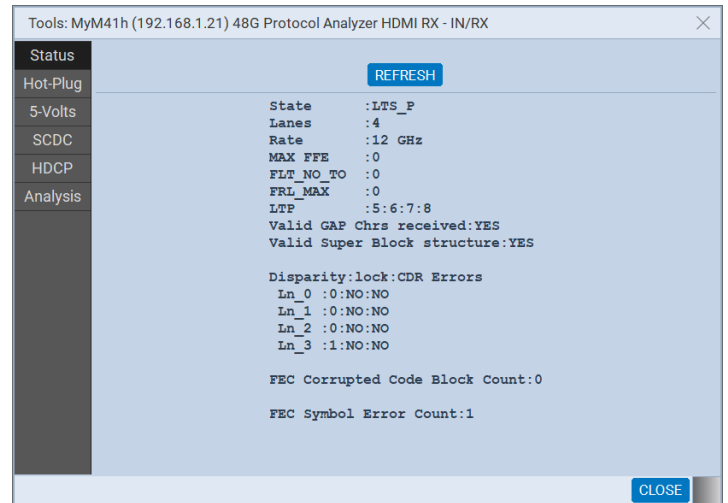


Test Setup for Source Test

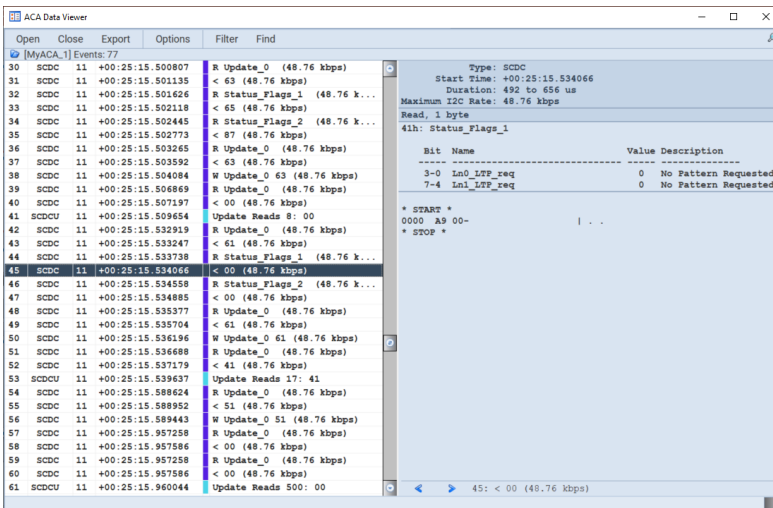
Auxiliary Channel Analyzer

You can use the 980 48G Protocol Analyzer / Generator module to monitor the Link Training transactions—EDID exchange and reads and writes to the SCDC registers over the DDC channel—with the Aux Channel Analyzer (ACA) utility. This enables you to verify link training functions to identify potential interoperability problems.

Analyzer Link Training Status Screen



Auxiliary Channel Analyzer (Link Training over DDC)



FIXED RATE LINK (FRL) VIDEO GENERATION

FRL Video Generation

The 980 48G module for HDMI® Testing enables developers of HDMI and TMDS FRL-capable sink devices and silicon makers to run functional tests on their FRL-capable display devices by rendering uncompressed, unencrypted or encrypted FRL streams at up to 8K and 10K video resolutions at lane rates up to 12Gb/s and at an aggregate link rate of 48Gb/s. The enhanced video generator function enables specific selections of video formats, colorimetry, bit depth, chroma subsampling, color space and test patterns.

HDMI 2.1 FRL-Capable UHD TV



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HDMI cable

Link Training Configuration

The 980 48G Protocol Analyzer / Generator module's video generation function enables you to configure the lane rate and number of lanes for transmission of the FRL stream.

EDID Read

The 980 48G Protocol Analyzer / Generator module enables you to view the EDID of the connected display (below). You can page through each block and save for later viewing.

Reading the EDID

EDID Decode Read Save Load Edit
Block #01
EDID Comp CTA Data Block: Tag 3, bytes 7: Vendor Specific
24-bit IEEE Registration ID: 0x045D08
HDMI Forum Vendor Specific Data Block
* Version: 1
* Max TMDS Character_Rate: 600 MHz
* Max FRL Rate: 12 Gbps @ 4 Lanes

Y:	SCDC_Present
N:	RR_Capable
N:	CABLE_STATUS
N:	CDC_PCT
Y:	LTE_34MHz_scramble
N:	Independent_view
N:	Dual_View
N:	3D_OSD_Disparity
N:	UHD_VIC
Y:	DC_48bit_420
Y:	DC_36bit_420
Y:	DC_30bit_420

Selection of FRL and TMDS Video Resolutions

Resolution	VESA	Folder	Lists	EDID	Frame Rate	Aspect Ratio
240p2x	240p4x	262	263		24/1.001	24
288p2x	288p4x	312	313			25
480p		314			30/1.001	30
480p2x	480i2x				48/1.001	48
480p4x	480i4x					50
576p					60/1.001	60
576p2x	576i2x					100
576p4x	576i4x				120/1.001	120
720p						200
1080p	1080i	1125	1250		240/1.001	240
2160p	4320p					240

Link Training Configuration

Force Link Train at

- Lane / Rate
- FRL Off
- 3 Lanes / 3 Gbps
- 3 Lanes / 6 Gbps
- 4 Lanes / 6 Gbps
- 4 Lanes / 8 Gbps
- 4 Lanes / 10 Gbps
- 4 Lanes / 12 Gbps

Auxiliary Channel Analyzer (ACA)

You can use the 980 48G Protocol Analyzer / Generator module to monitor the Link Training transactions—EDID exchange and reads and writes to the SCDC registers over the DDC channel—with the Aux Channel Analyzer utility. The FRL link training transactions enable developers to verify that their displays are properly conducting their role in the link training process.

Auxiliary Channel Analyzer (Link Training)

ACA Data Viewer

Open Close Export Options Filter Find

[MyACA_1] Events: 77

Time	Event	Value
30	SCDC	11 +00:25:15.500807 R Update_0 (48.76 kbps)
31	SCDC	11 +00:25:15.501135 < 63 (48.76 kbps)
32	SCDC	11 +00:25:15.501626 R Status_Flags_1 (48.76 kbps)
33	SCDC	11 +00:25:15.502118 < 65 (48.76 kbps)
34	SCDC	11 +00:25:15.502445 R Status_Flags_2 (48.76 kbps)
35	SCDC	11 +00:25:15.502773 < 87 (48.76 kbps)
36	SCDC	11 +00:25:15.503265 R Update_0 (48.76 kbps)
37	SCDC	11 +00:25:15.503592 < 63 (48.76 kbps)
38	SCDC	11 +00:25:15.504084 W Update_0 63 (48.76 kbps)
39	SCDC	11 +00:25:15.506869 R Update_0 (48.76 kbps)
40	SCDC	11 +00:25:15.507197 < 00 (48.76 kbps)
41	SCDC	11 +00:25:15.509654 Update Reads 8: 00
42	SCDC	11 +00:25:15.539199 R Update_0 (48.76 kbps)
43	SCDC	11 +00:25:15.533247 < 61 (48.76 kbps)
44	SCDC	11 +00:25:15.533738 R Status_Flags_1 (48.76 kbps)
45	SCDC	11 +00:25:15.534066 < 00 (48.76 kbps)
46	SCDC	11 +00:25:15.534558 R Status_Flags_2 (48.76 kbps)
47	SCDC	11 +00:25:15.534885 < 00 (48.76 kbps)
48	SCDC	11 +00:25:15.535377 R Update_0 (48.76 kbps)
49	SCDC	11 +00:25:15.535704 < 61 (48.76 kbps)
50	SCDC	11 +00:25:15.536196 W Update_0 61 (48.76 kbps)
51	SCDC	11 +00:25:15.536688 R Update_0 (48.76 kbps)

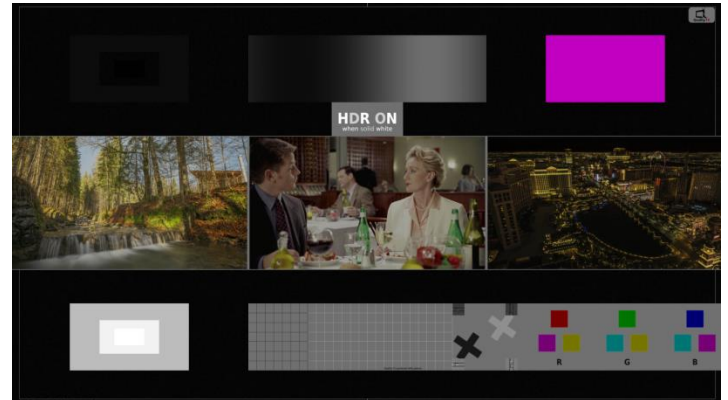
HDR FUNCTIONAL TESTING – HDR LAB, DOLBY VISION, HLG

HDR Lab

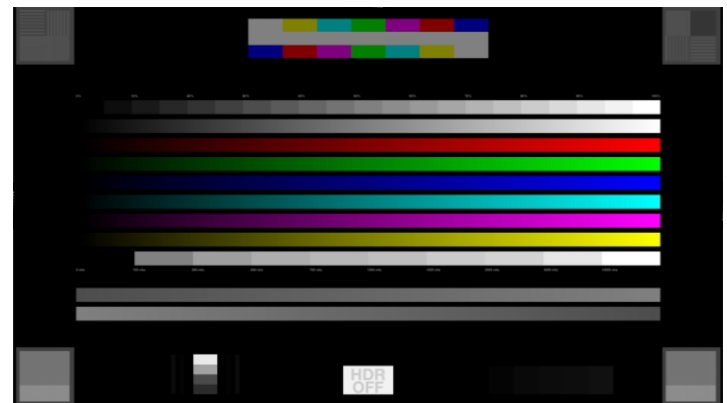
The “HDR Lab” test option was developed jointly with industry expert Joe Kane. HDR Lab is a suite of 4K and 8K test patterns and reference images for evaluating HDR10 displays (examples at right) that address the following:

- HDR End-to-End Validation in Post Production – Verifies HDR metadata, color grading and color decoding throughout the post production process.
- HDR Display Test Suite – Verifies various HDR attributes such as: peak brightness, native contrast, average brightness level, signal clipping, and color gamut on an HDR-capable UHD TV using a variety of test patterns.

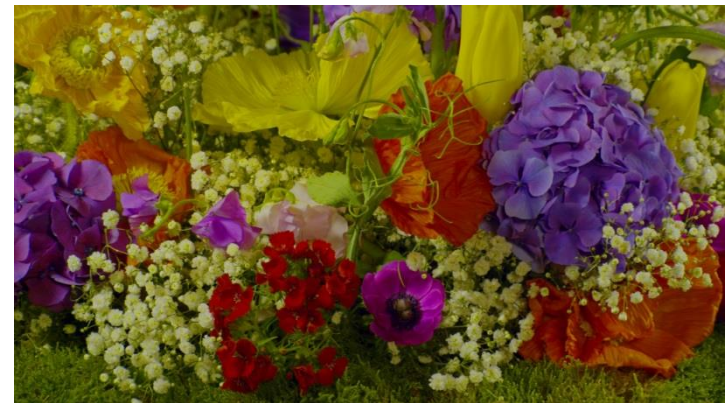
HDR Lab (Sample Test Pattern - Combination)



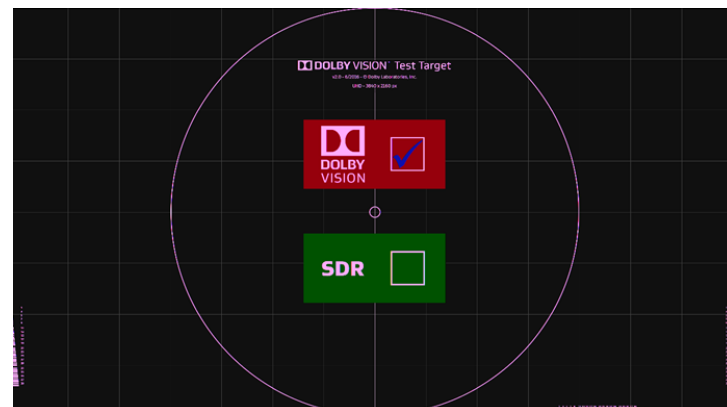
HDR Lab (Sample – Universal Test Pattern)



HDR Lab (Sample Test Pattern – Flower Montage)



Dolby Vision Test Image



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HDMI UHD TV



Setup for HDR Functional Tests

Dolby Vision & Hybrid Log Gamma Test Pattern

The Dolby Vision test image verifies a Dolby Vision display's Dolby Vision-specific EDID data, its response to the Dolby Vision protocol handshake and its handling of the Dolby Vision signal and metadata. The Dolby Vision test image will be rendered with a checkmark in the proper location if the display has properly interpreted the color space, metadata and checksum correctly.

The Hybrid Log Gamma (HLG) test image provides an assurance that the HLG metadata is not impeding the ability of the display to render the image.

HLG Test Image



FIXED RATE LINK (FRL) SOURCE COMPLIANCE

FRL & DSC Source Compliance Testing

The 980 48G module for HDMI® Testing enables developers of HDMI FRL-capable source devices and silicon makers to run compliance tests on their FRL-capable source devices on unencrypted FRL streams at up to 8K and 10K video resolutions at lane rates up to 12Gb/s and at an aggregate link rate of 48Gb/s. All compliance test data, including the captured data, is exportable and can be disseminated to colleagues and other subject matter experts.

980 with 48G Protocol Analyzer / Generator module for HDMI Testing

HDMI 2.1 Source

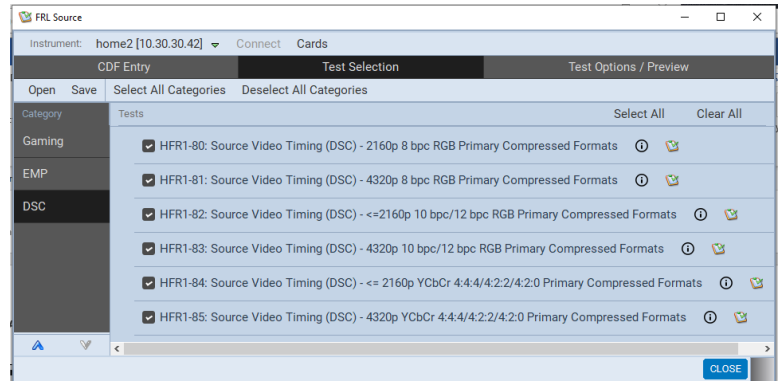


Test Setup for Source Test

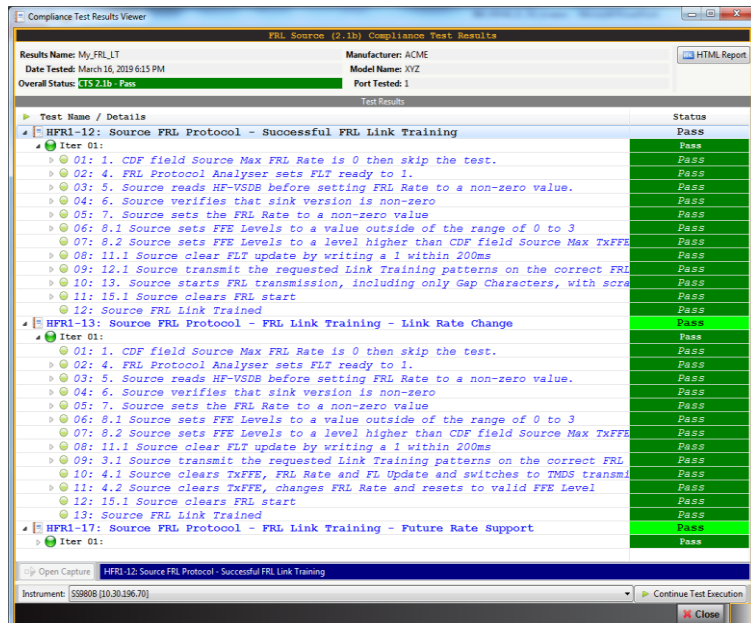
Selection of FRL Source Compliance tests



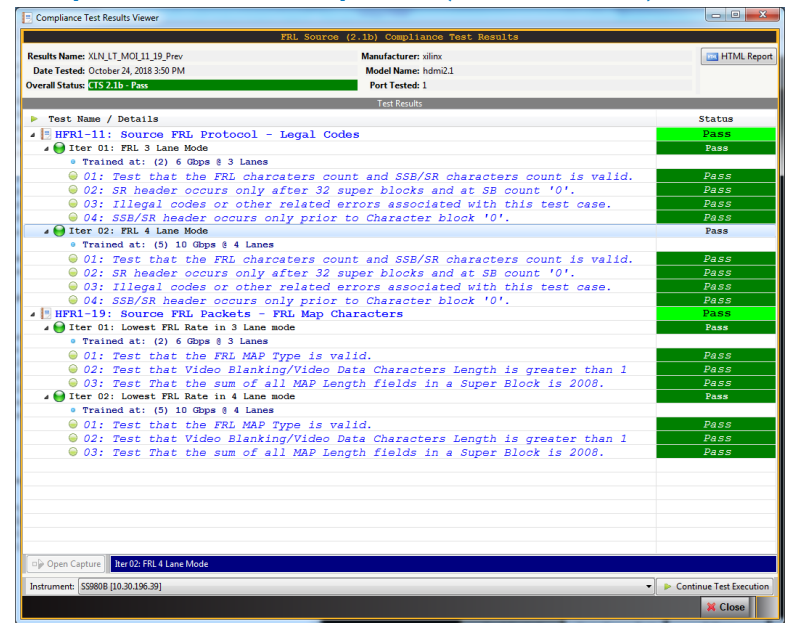
Selection of FRL DSC Source Compliance tests



Sample FRL Source Compliance (Link Training Tests)



Sample FRL Source Compliance (Protocol Tests)



FIXED RATE LINK (FRL) & DSC SINK COMPLIANCE

FRL & DSC Sink Compliance Testing

The M41h for HDMI Testing enables developers of HDMI® FRL and DSC-capable sink devices and silicon makers to run compliance tests on their FRL-capable sink devices with FRL streams at up to 8K and 10K video resolutions at lane rates up to 12Gb/s and at an aggregate link rate of 48Gb/s. All compliance test data, including the captured data, is exportable and can be disseminated to colleagues and other subject matter experts. The test patterns and formats necessary to run the DSC sink compliance tests are pre-cached for fast rendering.

Selection of FRL Sink & DSC Compliance tests

Protocol	Test Selection	Test Options / Preview
Protocol		
▼ HFR1-11: Source FRL Protocol - Legal Codes		
• Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)		
▼ HFR1-19: Source FRL Packets - FRL Map Characters		
• Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)		
▼ HFR1-20: Source FRL Packets - FRL Control Periods		
• Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)		
▼ HFR1-21: Source FRL Packets - Active Video FRL Packets (Uncompressed)		
• Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)		
▼ HFR1-23: Source FRL Protocol - Data Flow Metering Variations		
• Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)		
Link Training		
▼ HFR1-10: Source FRL Protocol - FRL Link Training Patterns		
• Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)		
▼ HFR1-12: Source FRL Protocol - Successful FRL Link Training		
• Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)		
▼ HFR1-13: Source FRL Protocol - FRL Link Training - Link Rate Change		
• Iter 01: Source_Max_FRL_Rate < 2: Automatic PASS(SKIP)		
▼ HFR1-17: Source FRL Protocol - FRL Link Training - Future Rate Support		
• Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)		
8bpc Encoding		
▼ HFR1-29: Source Pixel Encoding (FRL Mode) - RGB		
• Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)		
▼ HFR1-30: Source Pixel Encoding (FRL Mode) - YCBCR 4:2:2/4:4:4		
• Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)		
▼ HFR1-31: Source Pixel Encoding (FRL Mode) - YCBCR 4:2:0		
• Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)		

980 with 48G Protocol Analyzer / Generator



HDMI 2.1 (UHD TV)



HDMI cable

Test Setup for Sink Test

Sample DSC Sink Compliance Test Results

Test Name / Details	Pass	Fail
Iter 05: (196) 7680x4320p @ 30 Hz 16:9, RGB, 10 bpc		FAIL
• Step 2.1, 2.2: Format is in the EDID and CDF		
• Step 2.3: CDF field Sink_Supports_DSC matches the DSC_1p2 EDID field		
• Step 2.4: CDF field Sink_DSC_10bpc matches the DSC_10bpc EDID field		
• Step 2.4: CDF field Sink_DSC_12bpc matches the DSC_12bpc EDID field		
• Step 2.5: DSC_16bpc field in the EDID is not set (=0)		
• Step 2.6: CDF field Sink_DSC_Native_420 matches the DSC_Native_420 EDID field		
• 01: 6 Gbps @ 3 Lanes, MIN Pixel Clock	PASS	
• 02: 6 Gbps @ 3 Lanes, MAX Pixel Clock	FAIL	
• Manual inspection of the DUT indicated inadequate support of the test signal.		
• 03: 12 Gbps @ 4 Lanes, MIN Pixel Clock	PASS	
• 04: 12 Gbps @ 4 Lanes, MAX Pixel Clock	PASS	
• Manual inspection of the DUT verified adequate support of the test signal.		
Iter 06: (196) 7680x4320p @ 30 Hz 16:9, RGB, 12 bpc		PASS
• Step 2.1, 2.2: Format is in the EDID and CDF		
• Step 2.3: CDF field Sink_Supports_DSC matches the DSC_1p2 EDID field		
• Step 2.4: CDF field Sink_DSC_10bpc matches the DSC_10bpc EDID field		
• Step 2.4: CDF field Sink_DSC_12bpc matches the DSC_12bpc EDID field		
• Step 2.5: DSC_16bpc field in the EDID is not set (=0)		
• Step 2.6: CDF field Sink_DSC_Native_420 matches the DSC_Native_420 EDID field		
• 01: 6 Gbps @ 3 Lanes, MIN Pixel Clock	PASS	

Sample Test Results of FRL Sink Compliance tests

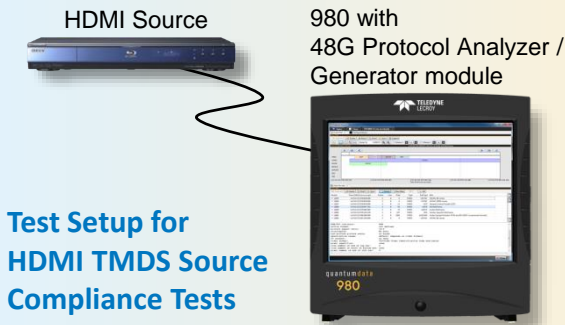
Test Name / Details	Pass	Fail
Iter 01: 3 Lanes		FAIL
• 01: 1. CDF field Source Max FRL Rate is 0 then skip the test.		
• 02: 4. Read the RS0C, verify that RS C Valid flag = 0; otherwise FAIL.		
• 03: 7. Read each FRL Look bit. Repeat until all FRL Look bits are set (=1) on all active Lanes, else FAIL after 10 milliseconds.		
• 04: 8. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 10 milliseconds.		
• 05: 10. Read the RS0C, verify that RS C Valid flag = 1 and count = 0 or 1; otherwise FAIL.		
• 06: 11. Corrupt symbols at a rate of about 1e-9, spaced out over 10 seconds, with 1 symbol per 100 milliseconds.		
• 07: 12. Read the RS0C; if the value is not correct within 1 count then FAIL.		
• 08: 13. Read the RS0C again after 100 milliseconds; if the count is not 0 or 1 then FAIL.		
• 09: 14. Corrupt symbols at a rate of about 2e-9, spaced out over 10 seconds, with 2 symbols per 100 milliseconds.		
• 10: 15. Read the RS0C; if the value is not correct within 1 count then FAIL.		
• 11: 16. Corrupt one symbol in each of 4 consecutive RS blocks, after generating the FRL data stream to be random data on all lanes.		
• 12: 17. Change the FRL data stream to be random data on all lanes.		
• 13: 18. After 3 seconds, read each FRL Look bit and verify that they have all been cleared (=0).		
• 14: 19. Read the RS0C, verify that RS C Valid flag = 1; otherwise FAIL.		
• 15: 20. If the count in the RS0C is less than 4, then FAIL.		
Iter 02: 4 Lanes		FAIL
• 01: 1. CDF field Source Max FRL Rate is 0 then skip the test.		
• 02: 2. Perform Link Training at the minimum FRL Rate with the maximum number of FRL lanes.		
• 03: 4. Read each FRL Look bit. Repeat until all FRL Look bits are set (=1) on all active Lanes, then FAIL.		
• 04: 7. Read the RS0C, verify that RS C Valid flag = 1 and count = 0 or 1; otherwise FAIL.		
• 05: 8. Corrupt one symbol in each of a known random number (between 10000 and 30000) of 100 milliseconds after the start of the symbol error, read the RS0C and verify that the count is outside the range of 12 from the number of good symbols.		
• 06: 9. Write a 1 to the RS0D Update bit to reset the flag.		
• 07: 11. If the corruption count is outside the range of 12 from the number of good symbols, then FAIL.		
Iter 03: Sink FRL Protocol - RS - Correction Counting During Reads		FAIL
• 01: 1. CDF field Source Max FRL Rate is 0 then skip the test.		
• 02: 2. Perform Link Training at the minimum FRL Rate with the maximum number of FRL lanes.		
• 03: 4. Read each FRL Look bit. Repeat until all FRL Look bits are set (=1) on all active Lanes, then FAIL.		
• 04: 7. Read the RS0C, verify that RS C Valid flag = 1 and count = 0 or 1; otherwise FAIL.		
• 05: 8. Write a 1 to the RS0D Update bit to reset the flag.		
• 06: 10. Corrupt one symbol in each of 32768 RS blocks over a 14-second period at the minimum FRL Rate.		
• 07: 11. Read the RS0D Update flag, verify that it has been set to a 1.		
• 08: 13. Read the RS0D Update flag, verify that it is cleared to 0.		

Test Name / Details	Pass	Fail
Iter 01: 3 Lanes		FAIL
• 01: 1. CDF field Source Max FRL Rate is 0 then skip the test.		
• 02: 2. Read the EDID after NPD is asserted.		
• 03: 3. Read each FRL Look bit after 10 milliseconds. If any FRL Look bits are cleared (=0) on any active Lanes, then FAIL.		
• 04: 4. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 1 second.		
• 05: 6.1. Verify that each Error Counter has the Valid flag set (=1), else FAIL.		
• 06: 6.2. Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.		
• 07: 8.3. Verify that the Error Counter for any lane has an error count that is not 0 except first time then FAIL.		
• 08: 10.1. Read the FRL Look bit for each Lane, verify it is still set (=1).		
• 09: 10.2. Read the FRL Lane Error Counters for each active Lane in a single transaction, including the checksum byte at offset 0x56. Verify that the sum of the counters is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.		
• 10: 10.3. Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.		
Iter 02: 4 Lanes		FAIL
• 01: 1. CDF field Source Max FRL Rate is 0 then skip the test.		
• 02: 2. Read the EDID after NPD is asserted.		
• 03: 3. Read each FRL Look bit after 10 milliseconds. If any FRL Look bits are cleared (=0) on any active Lanes, then FAIL.		
• 04: 4. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 1 second.		
• 05: 6.1. Verify that each Error Counter has the Valid flag set (=1), else FAIL.		
• 06: 6.2. Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.		
• 07: 8.3. Verify that the Error Counter for any lane has an error count that is not 0 except first time then FAIL.		
• 08: 10.1. Read the FRL Look bit for each Lane, verify it is still set (=1).		
• 09: 10.2. Read the FRL Lane Error Counters for each active Lane in a single transaction, including the checksum byte at offset 0x56. Verify that the sum of the counters is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.		
• 10: 10.3. Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.		
Iter 03: Sink FRL Protocol - CED - Update Flag with Specific Error Injection		FAIL
• 01: 1. CDF field Source Max FRL Rate is 0 then skip the test.		
• 02: 2. Perform Link Training at the minimum FRL Rate with the maximum number of FRL lanes supported by the DUT.		
• 03: 4. Read each FRL Look bit after 10 milliseconds. If any FRL Look bits are cleared (=0) on any active Lanes, then FAIL.		
• 04: 7. Read the RS0C Update flag, verify it is set (=1). If the RS0C Update flag is not set, then FAIL.		
• 05: 7. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL.		
• 06: 11. Read the FRL CED Update flag, verify it is set (=1). If the CED Update flag is not set, then FAIL.		
• 07: 14. Read the FRL CED Update flag, verify it has been set (=1) again. If the CED Update flag is not set, then FAIL.		
• 08: 15. Read the FRL CED Update flag, verify it has been cleared (=0). If the CED Update flag is not cleared, then FAIL.		

HDMI 2.0 / 1.4 SOURCE/SINK TMDS COMPLIANCE TESTS

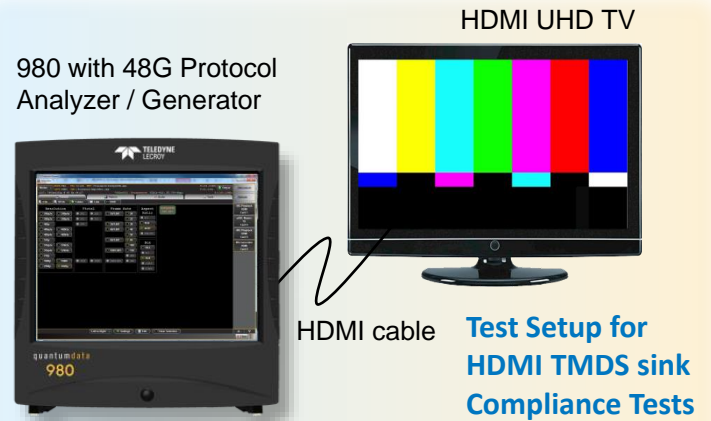
HDMI TMDS Source Compliance

The 980 48G module for HDMI® Testing enables developers of HDMI source devices and silicon makers to run compliance tests on their TMDS source devices on streams at up to 4K video resolutions. All compliance test data, including the captured data, is exportable and can be disseminated to colleagues and other subject matter experts. (Example screens below show samples only.)



HDMI TMDS Sink Compliance

The 980 48G module for HDMI Testing enables developers of HDMI sink devices and silicon makers to run compliance tests on their TMDS sink devices at up to 4K video resolutions. All compliance test data, including the captured data, is exportable and can be disseminated to colleagues and other subject matter experts.



HDMI TMDS Source – Partial List of Supported Tests

Select All	Duration	Options	EXECUTE TESTS
TMDS Protocol			
>	HF1-10: TMDS Protocol - 6G - TMDS Bit Clock Ratio		✓
>	HF1-11: Source TMDS Protocol - 6G Legal Codes		✓
>	HF1-12: TMDS Protocol - 6G - Basic Protocol and Scrambling		✓
>	HF1-13: TMDS Protocol - Scrambling <= 3.4Gbps		✓
>	HF1-21: TMDS Protocol - 6G - Legal Codes - other Video Timings		✓
>	HF1-22: TMDS Protocol - 6G - Basic Protocol and Scrambling - Other Video Timings		✓
Pixel Encoding			
>	HF1-31: Pixel Encoding - YCBCR 4:2:0 - TMDS Pixel Encoding		✓
>	HF1-32: Pixel Encoding - YCBCR 4:2:0 Deep Color - TMDS Pixel Encoding		✓
Video Timing			
>	HF1-14: Video Timing - 6G - 2160p 24-bit Color Depth		✗
>	HF1-15: Video Timing - 6G - Deep Color		✓
>	HF1-16: Video Timing - 6G - 2160p 3D		✓
>	HF1-24: Video Timing - 6G - Other 24-bit Color Depth		✓
>	HF1-25: Video Timing - 6G - Other Deep Color		✓
>	HF1-26: Video Timing - 6G - Non-2160p 3D		✓
>	HF1-33: Video Timing - YCBCR 4:2:0		✓
>	HF1-34: Video Timing - YCBCR 4:2:0 Deep Color		✓
>	HF1-35: Video Timing - 21:9 (64:27)		✓

HDMI TMDS Sink – Partial List of Supported Tests

Select All	EXECUTE TESTS
TMDS Protocol	
>	HF2-5: TMDS Protocol - 6G - Scrambling ✓
>	HF2-9: TMDS Protocol - Scrambling <= 340Mpsc ✓
Pixel Decoding	
>	HF2-23: Pixel Decoding - YCBCR 4:2:0 ✓
>	HF2-24: Pixel Decoding - YCBCR 4:2:0 Deep Color ✓
>	HF2-71: Pixel Decoding - YCBCR 4:2:0 for 861G Video Formats ✓
>	HF2-72: Pixel Decoding - YCBCR 4:2:0 Deep Color for 861G Video Formats ✓
EDID	
>	HF2-10: Video Timing - 6G - HF-VSDB ✓
>	HF2-26: EDID - Video Format Declaration ✓
>	HF2-31: EDID - YCBCR 4:2:0 - Data Blocks ✓
>	HF2-32: EDID - YCBCR 4:2:0 BT.2020 - Data Block ✓
>	HF2-35: EDID YCBCR 4:2:0 Deep Color HF-VSDB ✓
>	HF2-39: EDID 3D and Multi-stream Audio Data Blocks ✓
>	HF2-41: HDMI VSDBs - Independent-View ✓
>	HF2-53: EDID - HF-VSDB ✓
>	HFR2-53: Sink Video Timing - FRL/Gaming/DSC - HF-VSDB ✓
>	HFR2-70: Sink EDID - HF-VSDB Reserved Bits ✓
Timing 6G	
>	HF2-6: Video Timing - 6G - 2160p 24-bit Color Depth ✓
>	HF2-7: Video Timing - 6G - Deep Color ✓

HDMI TMDS Test Results – Video Tests

Test Name / Details	Status
HF1-25: Video Timing - 6G - Other Deep Color	
> Iter 01: (63) 1920x1080p @ 120 Hz, DC - 36 bpp	Pass
> Iter 02: (64) 1920x1080p @ 100 Hz, DC - 36 bpp	Pass
> Iter 03: (77) 1920x1080p @ 100 Hz, DC - 36 bpp	Pass
> Iter 04: (78) 1920x1080p @ 120 Hz, DC - 36 bpp	Pass
> Iter 05: (91) 2560x1080p @ 100 Hz, DC - 36 bpp	Pass
> Iter 06: Any non-2160p DC Format, Max TMDS check	Pass
HF1-18: AVI InfoFrames - 6G	
> Iter 01: (95) 3840x2160p @ 50 Hz	Pass
> Iter 02: (97) 3840x2160p @ 60 Hz	Pass
> Iter 03: (101) 4096x2160p @ 50 Hz	Pass
> Iter 04: (102) 4096x2160p @ 60 Hz	Pass
> Iter 05: (106) 3840x2160p @ 50 Hz	Pass
01: Verify AVI InfoFrame occurs at least once per two Video Fields	Pass
02: Verify AVI InfoFrame version is equal to 2	Pass
03: Verify AVI VIC is 0 for HDMI VICs	Pass
04: Verify AVI VIC is correct for non-HDMI VICs	Pass
05: Verify AVI PB1 bit 7 is 0	Pass
06: Verify AVI PB4 bit 7 is 0	Pass
07: Verify AVI PB14-PB27 bytes are 0	Pass
> Iter 06: (107) 3840x2160p @ 60 Hz	Pass
> Iter 07: (93) 3840x2160p @ 24 Hz, DC - 36 bpp	Pass
> Iter 08: (94) 3840x2160p @ 25 Hz, DC - 36 bpp	Pass
> Iter 09: (95) 3840x2160p @ 30 Hz, DC - 36 bpp	Pass

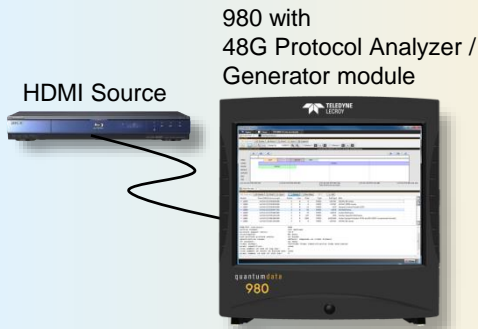
HDMI TMDS Test Results – Video Tests

Test Name / Details	Status
HF2-7: Video Timing - 6G - Deep Color	
> Iter 07: (93) 3840x2160p @ 24 Hz 16:9, 30 bpp	Pass
> Iter 08: (93) 3840x2160p @ 24 Hz 16:9, 36 bpp	Pass
> Iter 09: (93) 3840x2160p @ 24 Hz 16:9, 48 bpp	Skipped
> Iter 10: (94) 3840x2160p @ 25 Hz 16:9, 30 bpp	Pass
> Iter 11: (94) 3840x2160p @ 25 Hz 16:9, 36 bpp	Pass
> Iter 12: (94) 3840x2160p @ 25 Hz 16:9, 48 bpp	Skipped
> Iter 13: (95) 3840x2160p @ 30 Hz 16:9, 30 bpp	Pass
> Iter 14: (95) 3840x2160p @ 30 Hz 16:9, 36 bpp	Pass
> Iter 15: (95) 3840x2160p @ 30 Hz 16:9, 48 bpp	Skipped

HDCP 2.3 SOURCE, SINK, REPEATER COMPLIANCE TESTS

HDCP 2.3 Compliance (TMDS)

The 980 HDCP 2.3 compliance tests are ideal for pre-testing your HDMI® source, sink or repeater product prior to submission to an Authorized Test Center for approval. Pre-testing provides assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the auxiliary channel analyzer traces logged during the test to help diagnose the cause of compliance test failures. HDCP source test examples are shown.



Test Setup for HDCP Source Compliance Tests

HDCP 2.3 Test Selection – List of Source Tests

Instrument: MyM41h [192.168.1.21] Connect Cards

CDF Entry Test Selection Test Options / Preview

Select All EXECUTE TESTS

- TX with Receiver
 - 1A-01: Regular Procedure: With previously connected Receiver (With stored Km) ✓
 - 1A-02: Regular Procedure: With newly connected Receiver (Without stored Km) ✓
 - 1A-03: Regular Procedure: Receiver disconnect after AKE_Init ✓
 - 1A-04: Regular Procedure: Receiver disconnect after Km ✓
 - 1A-05: Regular Procedure: Receiver disconnect after locality check ✓
 - 1A-06: Regular Procedure: Receiver disconnect after Ks ✓
 - 1A-07: Regular Procedure: Receiver sends REAUTH_REQ after Ks ✓
 - 1A-08: Irregular Procedure: Rx certificate not received. ✓
 - 1A-09: Irregular Procedure: Verify Receiver Certificate ✓
 - 1A-10: Irregular Procedure: SRM
 - Iter 01: This test has been deprecated: Automatic Not Judged ✓
 - 1A-11: Irregular Procedure: Invalid H'
 - Iter 01: Invalid H' ✓
 - Iter 02: H' Timeout with previously paired Recv Id ✓
 - Iter 03: H' Timeout with previously unpaired Recv Id ✓
 - 1A-12: Irregular Procedure: Pairing Failure ✓
 - 1A-13: Irregular Procedure: Locality Failure
 - Iter 01: Locality Failure ✓
 - Iter 02: Locality Timeout ✓
- TX with Repeater
 - 1B-01: Regular Procedure: With Repeater ✓

CLOSE

HDCP 2.3 Test Results– Source Tests

Compliance Test Results Viewer

HDMI HDCP 2.3 TX (1.0) Compliance Test Results

Results Name: HDMI_HDCP_22_01 Manufacturer: HTML Report

Date Tested: January 28, 2015 9:39 AM Model Name:

Overall Status: CTS 1.0 - Fail Port Tested: 1

Test Name / Details	Status
1A-01: Regular Procedure: With previously connected Receiver	Pass
1A-02: Regular Procedure: With newly connected Receiver (With	Pass
1A-03: Regular Procedure: Receiver disconnect after AKE_Init	Pass
1A-04: Regular Procedure: Receiver disconnect after Km	Pass
1A-05: Regular Procedure: Receiver disconnect after locality	Pass
1A-06: Regular Procedure: Receiver disconnect after Ks	Pass
1A-07: Regular Procedure: Receiver sends REAUTH_REQ after Ks	Fail
1A-08: Irregular Procedure: Rx certificate not received.	Pass
Iter 01:	Pass
HPD Deasserted regular	
HPD Asserted regular	
RX:UNAUTH	
Warn:NO VIDEO Present	
INFO RK UNAUTH:Rep:0 Cnt:0 Depth:0	
MSG:VERSION ts:0x0 us	
MSG:Encryption disabled	
RCVD:AKE_Init ts:0x118cb0a us	
Test Cond. skipCert	
HDMI/VIDEO Present	
RCVD:AKE_Init ts:0x1314070 us	
Test Cond. ake_init	
Encryption Disabled	
1A-09: Irregular Procedure: Verify Receiver Certificate	Pass
1A-11: Irregular Procedure: Invalid H'	Pass
1A-12: Irregular Procedure: Pairing Failure	Pass
1A-13: Irregular Procedure: Locality Failure	Pass
1B-01: Regular Procedure: With Repeater	Pass
1B-02: Irregular Procedure: Timeout of Receiver ID list	Pass
1B-03: Irregular Procedure: Verify V'	Pass
1B-04: Irregular Procedure: MAX DEVS EXCEEDED	Pass
1B-05: Irregular Procedure: MAX CASCADE EXCEEDED	Pass
1B-06: Irregular Procedure: Incorrect seq num V	Pass
1B-07: Regular Procedure: Re-authentication on HDCP HPD	Pass
1B-08: Regular Procedure: Re-authentication on REAUTH_REQ	Fail
1B-09: Irregular Procedure: Rollover of seq num V	Pass
1B-10: Irregular Procedure: Failure of Content Stream Managem	Pass

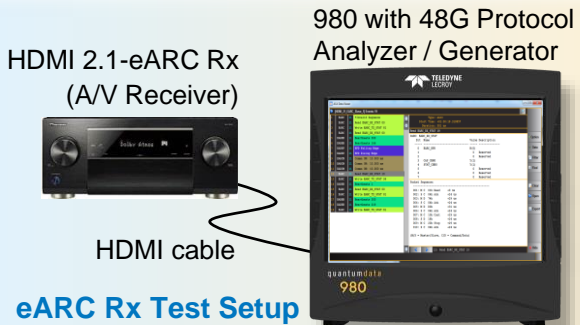
Instrument: PG980B [10.30.196.27] Continue Test Execution

CLOSE

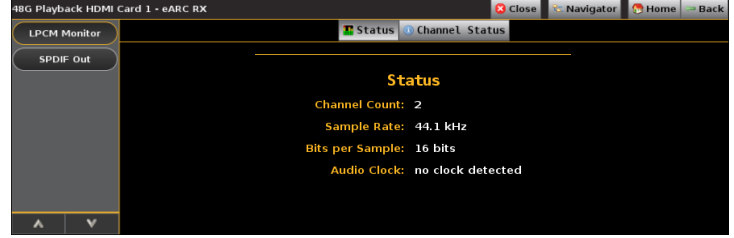
eARC FUNCTIONAL AND COMPLIANCE TESTING

eARC Functional Testing

The 980 48G module is also supports enhanced Audio Return Channel (eARC) Tx/Rx functional testing. The solution provides emulation of an eARC Tx and Rx functions over the eARC Common Mode and Differential mode data channels. Solution supports discovery and disconnect, heartbeat, status and capabilities data structure and transmission over the differential channel. (Sample screen showing monitoring incoming audio stream, right.)

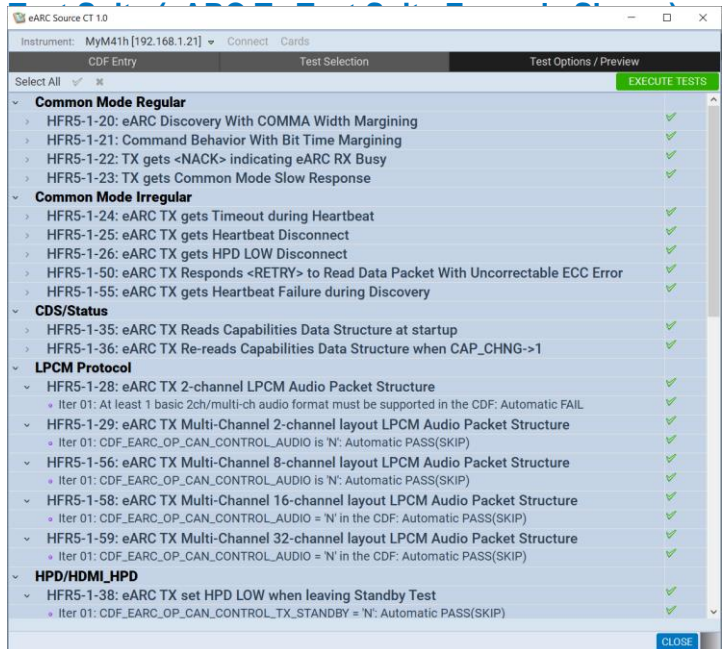
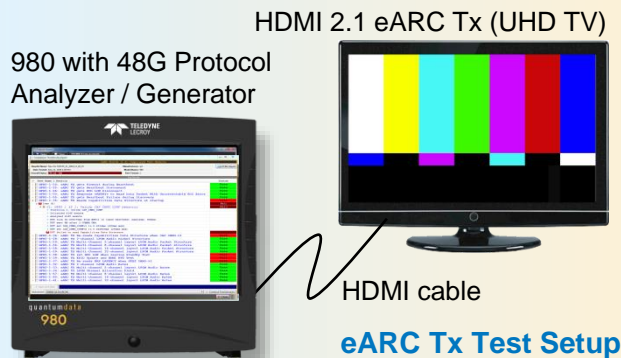


eARC Rx Test Functional Testing



eARC Compliance Testing

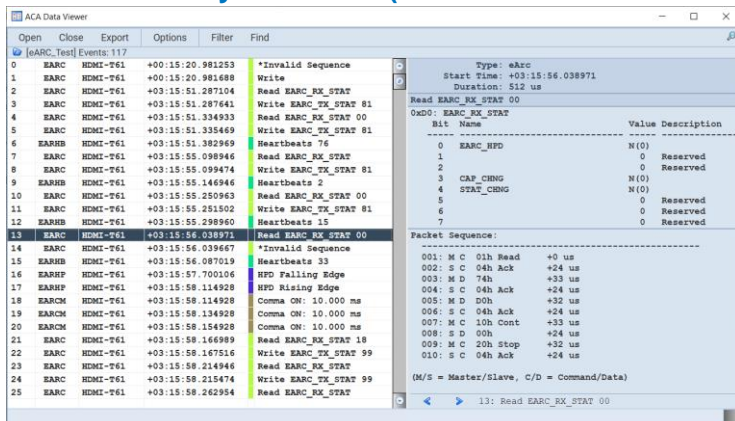
The 980 48G module enables developers of HDMI® eARC Tx and Rx devices to run compliance tests on their eARC-capable. The compliance tests run with little or no human interaction. Detailed results are provided for each test to help identify the root cause of failures. The reports can be exported and disseminated to colleagues and other subject matter experts.



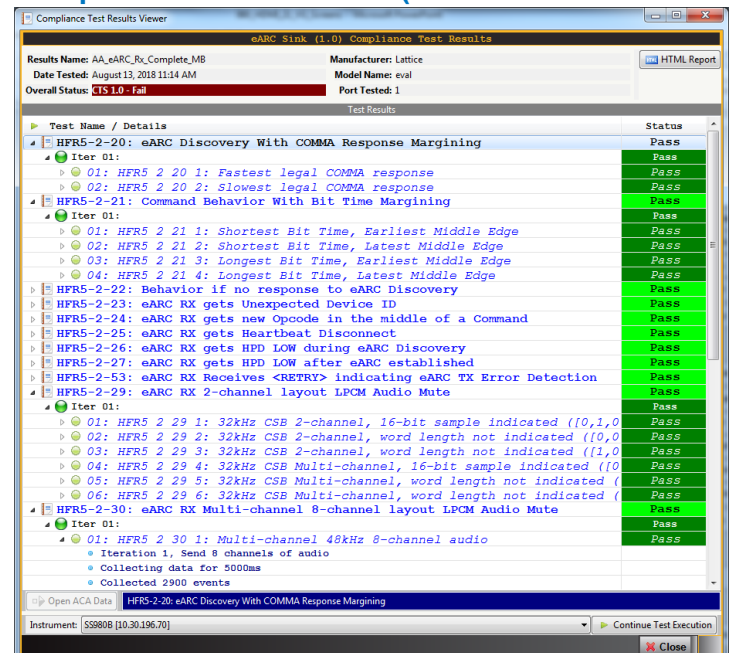
Auxiliary Channel Analyzer (ACA)

The 980 48G module can monitor the Link Training transactions—EDID exchange and reads and writes to the SCDC registers over the DDC channel -with the Aux Channel Analyzer (ACA) utility. Viewing the FRL link training transactions enables developers to verify their displays are properly conducting the link training process properly.

Aux Chan Analyzer Traces (Common Mode Discovery)



Sample eARC Test Results (eARC Rx Tests)



DISPLAY STREAM COMPRESSION (DSC) TESTING

Display Stream Compression Video Generation

The 980 48G module enables developers of HDMI® DSC-capable sink devices and silicon makers to run Display Stream Compression (DSC) functional and compliance tests on their FRL-capable display devices by rendering compressed, unencrypted or encrypted FRL streams at up to 8K video resolutions at lane rates up to 12Gb/s. The test patterns and formats necessary to run the DSC sink compliance tests are pre-cached for fast rendering.

Display Stream Compression Video Analysis

The 980 48G module enables developers of HDMI DSC-capable source devices and silicon makers to run Display Stream Compression (DSC) functional and compliance tests on their FRL-capable source devices by rendering compressed, unencrypted or encrypted FRL streams at up to 8K video resolutions at lane rates up to 12Gb/s. There is a new "No Video" mode that enables you quickly verify the incoming DSC timing and metadata. You can then choose to view the uncompressed video frames.

DSC Real Time Analysis



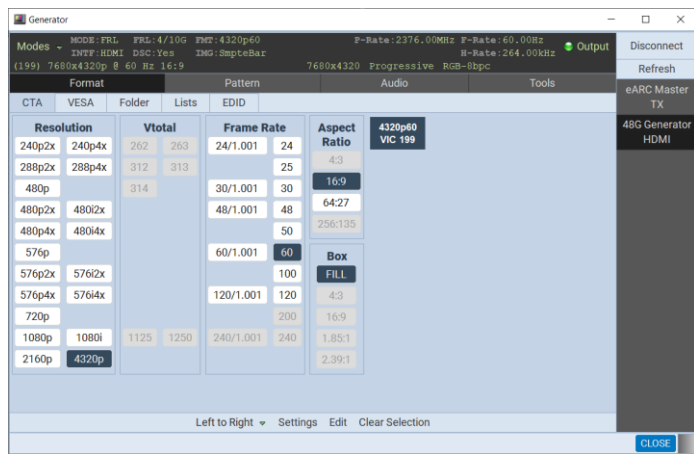
HDMI FRL, DSC-Capable UHD TV

980 with 48G Protocol Analyzer / Generator module for HDMI Testing

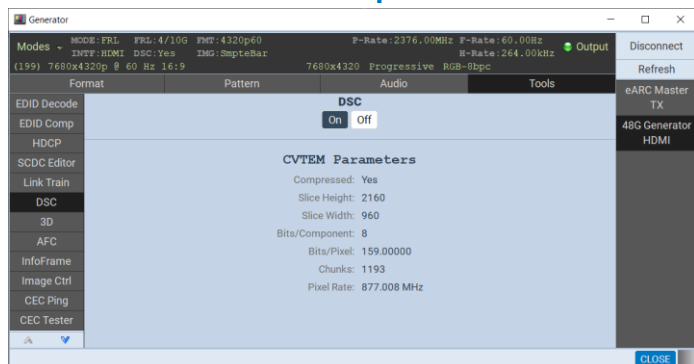


HDMI cable

DSC Video Generation Selection

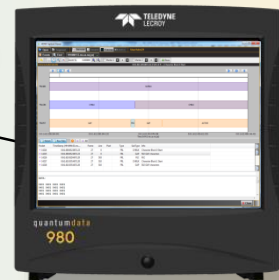


DSC Video Generation Setup



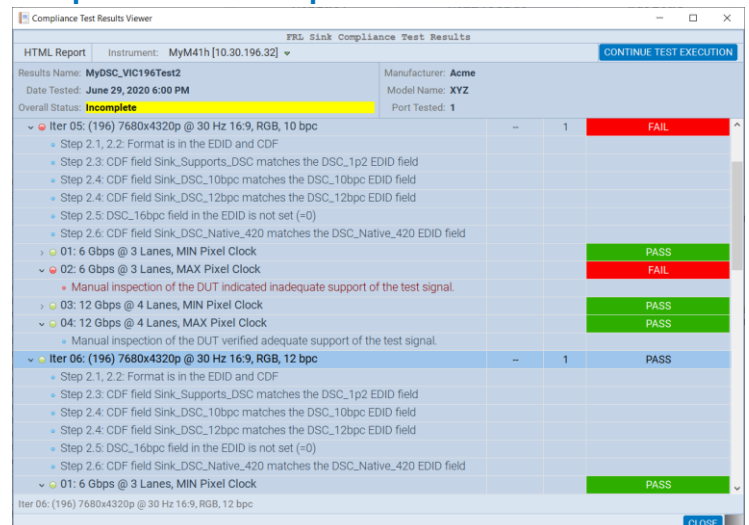
980 with 48G Protocol Analyzer / Generator module for HDMI Testing

HDMI 2.1 Source



Test Setup for Source Test

Sample DSC Sink Compliance Test Results



HDMI Ports

Version	HDMI® 2.1a
Standard Formats	CEA, VESA
Connector	Rx HDMI Type A; Category 2 Tx HDMI Type A; Category 2 Note: Connectors are not approved Category 3 connectors.
Protocols	FRL with FEC, DSC; HDCP 2.3, TMDS
FRL bit rates	3Gbps; 6Gbps; 8Gbps; 10Gbps; 12Gbps (48Gbps aggregate).
Max Resolution	up to 8K and 10K with DSC compression
Line Code	16b/18b
HDCP	HDCP 1.4 and 2.3
Capture memory	8 GBytes

HDMI 2.1 Protocol Analyzer Features

Fixed Rate Link (FRL)	Captures and Decodes Fixed Rate Link (FRL) and FEC data streams
Forward Error Correction	Displays FEC packets in FRL Character Blocks
FRL Lanes	3 & 4 lane configurations are supported
FRL Link Training Patterns	Supports LTP5 through LTP8
FRL Link Training	Supports link training with an FRL source in accordance with states defined in the HDMI 2.1 specification

HDMI 2.1 Video Generator Features

Fixed Rate Link (FRL)	Transmits Fixed Rate Link (FRL), FEC data streams and TMDS streams.
FRL Lanes	3 & 4 lane configurations are supported
FRL Link Training Patterns	Supports LTP5 through LTP8
FRL Link Training	Supports link training with an FRL sink in accordance with states defined in the HDMI 2.1 specification

HDMI 2.1 Module Options

Video Generator license	Transmits Fixed Rate Link (FRL) and FEC data streams and TMDS streams
Protocol Analysis license	Analyzes Fixed Rate Link (FRL) and FEC data streams and TMDS streams
Passive DDC monitoring	Passive DDC monitoring in FRL mode (requires custom cable)
Functional test for HDR Lab	HDR Lab test patterns and images for testing HDR10 updated for 8K
Functional test for eARC Tx	Emulate eARC Rx to run tests on an eARC Tx common & differential modes
Functional test for eARC Rx	Emulate eARC Tx to run tests on an eARC Rx common & differential modes
Compliance for eARC Tx	Run full compliance test on an eARC Tx (all tests supported) Note: HF5-1-51 test requires 980 18G Video Generator which has been discontinued
Compliance for eARC Rx	Run full compliance test on an eARC Rx (all tests supported)
Functional & Comp. DSC source tests	Run functional & compliance tests for Display Stream Compression sources
Functional & Compliance DSC sink	Run functional & compliance tests for Display Stream Compression sinks
Compliance FRL sources	Run full suite of FRL source compliance tests.
Compliance FRL & DSC sinks	Run full suite of FRL & DSC sink compliance tests
Compliance TMDS sources	Run full suite of TMDS source compliance tests
Compliance TMDS sink	Run full suite of TMDS sink compliance tests
Compliance HDCP 1.4 sources	Run full suite of HDCP 1.4 source compliance tests
Compliance HDCP 2.3 sinks	Run full suite of HDCP 2.3 sink compliance tests
Compliance HDCP 2.3 sources	Run full suite of HDCP 2.3 source compliance tests
Compliance HDCP 2.3 repeater	Run full suite of HDCP 2.3 repeater compliance tests

980B Test Platform

Embedded Display	15" diagonal; Resolution: 1024(H); x 768 (V) resolution; 24-bit RGB color
Power	90-264 VAC, 47-63Hz
Weight	23.76 LBS; 10.78 Kg
Size	Height: 15.25 in. (38.7 cm) Width: 14.57 in. (36.5 cm) Depth: 6.29 in. (15.9 cm)
Command Line Control	Ethernet (RJ-45) for external GUI and telnet
Environmental	Operating Temp: 32 to 90 (F); 0 to 32 (C)

